Bolt Schematic

Whiskey Lake

2018/12/13

REV : A00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed
TypeC: CCG4
TypeC_5V_OUT: provide external device power 5V
TypeC_PWR_IN: Provide system power via typeC connector.
8111H:Reltek LAN RTL811H
81106E:Reltek LAN RTL8106E

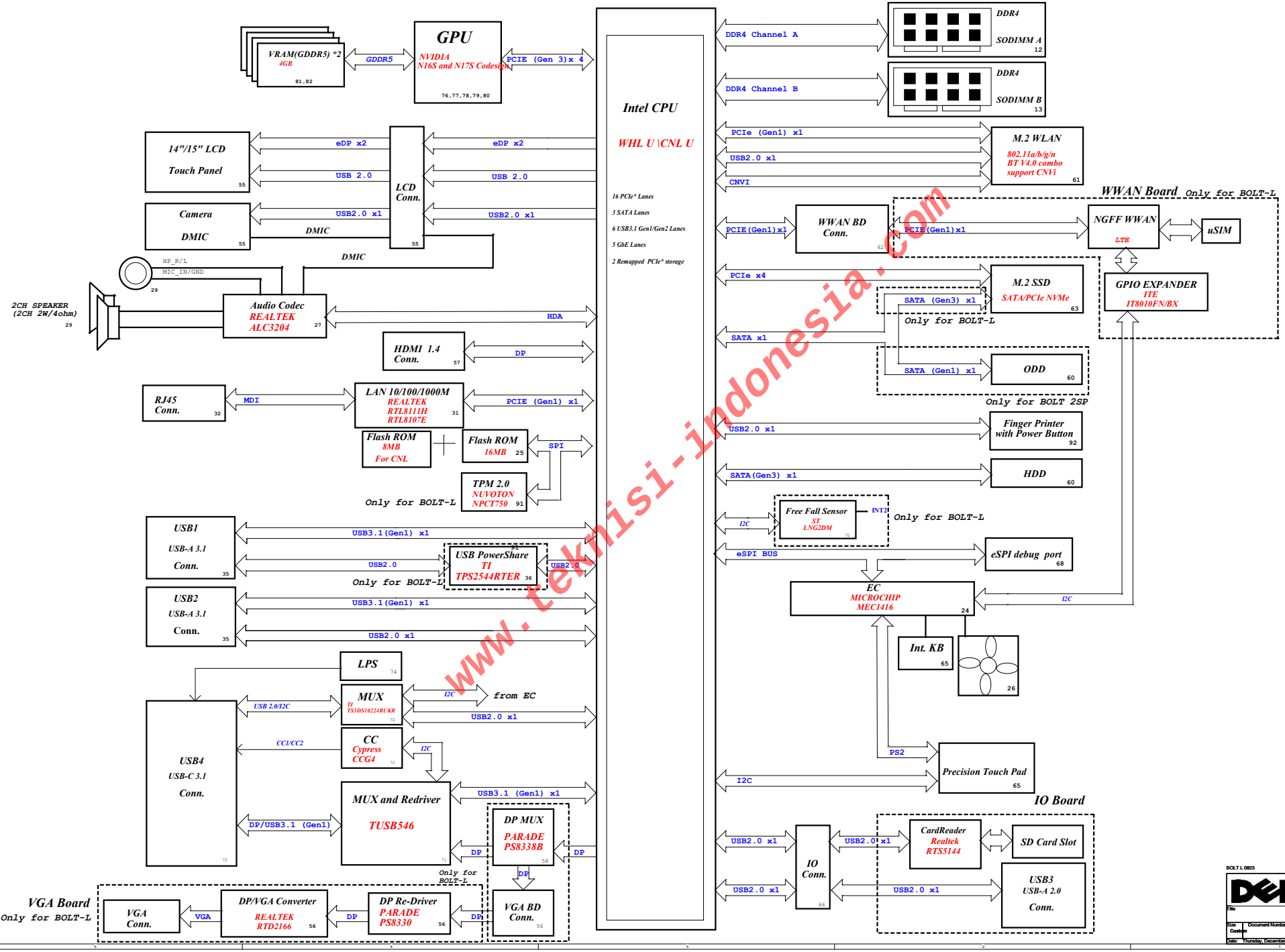
BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
Size: A3	Document Number: BOLT WHL	Rev: A00
Date: Thursday, December 27, 2018	Sheet 1 of 105	

Project Code : 4PD0G7010001
PCB P/N : 18763
Revision : SD

Bolt WHL Block Diagram



CHARGER		
ISL88739		44
INPUTS	OUTPUTS	
AD+ BT+	DCBATOUT	

SYSTEM DC/DC		
TPS51225RUKR-GP		45
INPUTS	OUTPUTS	
DCBATOUT	3D3V_PWR 3D3V_S5 5V_PWR 5V_S5	

CPU Core Power		
NCP81208MNTXG NCP81382MNTXG x 2 NCP81382MNTXG (23e) NCP81253MNTBG		46~50
INPUTS	OUTPUTS	
DCBATOUT DCBATOUT DCBATOUT DCBATOUT	VCC_CORE +VCCGT +VCCGT (23e) +VCCSA	

DDR4 SUS		
RT8231AGQW-GP APL5930KAI-TRG		51
INPUTS	OUTPUTS	
DCBATOUT 3D3V_S5	1D2V_S3 0D6V_S0 2D5V_S3	

CPU VCCPRIM_CORE 1V		
		11
INPUTS	OUTPUTS	
1D0V_S5	+VCCPRIM_CORE	

CPU DCDC-V1D00A		
AOZ2262QI-10-GP-U		53
INPUTS	OUTPUTS	
DCBATOUT	1D0V_S5	

LDO-V1D8V		
APL5930KAI-TRG		54
INPUTS	OUTPUTS	
3D3V_S5	1D8V_S5	

5V/3V S0		
TPS22966DPUR-GP		40
INPUTS	OUTPUTS	
5V_S5 3D3V_S5	5V_S0 3D3V_S0	

EOPIO/EDRAM (23e)		
TPS22961DNYT		40
INPUTS	OUTPUTS	
1D0V_S5 1D0V_S5	+V_EDRAM_VR +V_EOPIO_VR	

3D3V VGA		
AO3419L		86
INPUTS	OUTPUTS	
3D3V_S0	3D3V_VGA_S0	

VGA_CORE		
ISL62771HRTZ-GP-U		85
INPUTS	OUTPUTS	
DCBATOUT	VGA_CORE	

1D5V_VGA_S0		
Y8288RAC-GP		86
INPUTS	OUTPUTS	
DCBATOUT	1D5V_VGA_S0	

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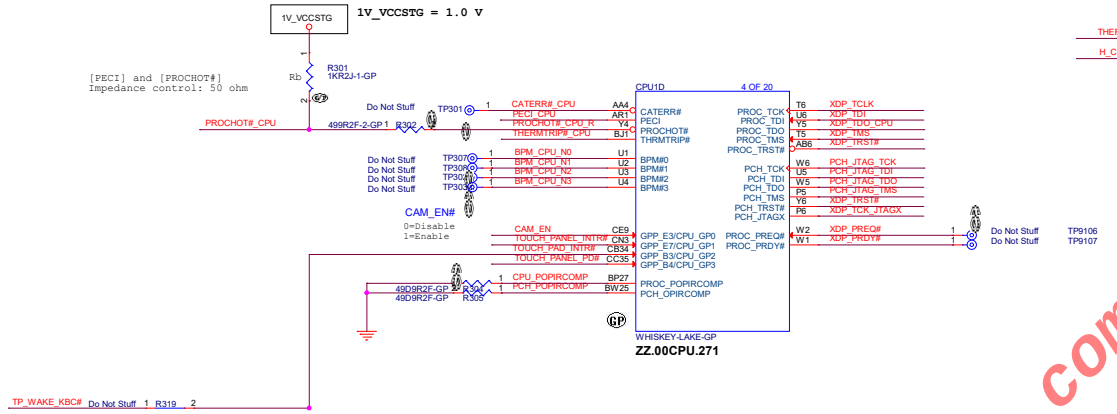
Title: Block Diagram
Size: Custom | Document Number: BOLT WHL | Rev: A00
Date: Thursday, December 27, 2018 | Sheet 2 of 105

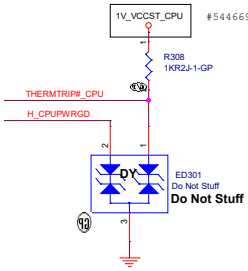
Main FUNC = CPU

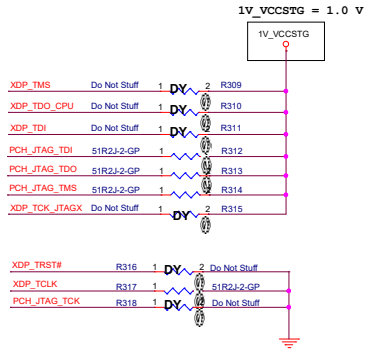
24 PECI_CPU
24,44,46 PROCHOT#_CPU
55 TOUCH_PANEL_INTR#
24,65 TP_WAKE_KBC#
55 TOUCH_PANEL_PD#
17 H_CPUPWRGD

55 CAM_EN

89 PCH_JTAG_TCK







(#575412) PROCHOT# Routing Guidelines

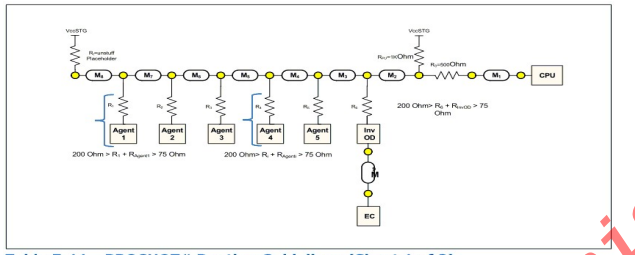


Table 7-11. PROCHOT# Routing Guidelines (Sheet 1 of 2)

Segment	Tline Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS	2	38	305	1495.06	12007.9
M2	MS/SL/DSL	VSS	2	279		10984.3	
M3	MS/SL/DSL	VSS	1	76		2992.13	
M4	MS/SL/DSL	VSS	1	76		2992.13	
M5	MS/SL/DSL	VSS	1	76		2992.13	
M6	MS/SL/DSL	VSS	1	76		2992.13	
M7	MS/SL/DSL	VSS	1	76		2992.13	
M8	MS/SL/DSL	VSS	1	8		341.96	
M9	MS/SL/DSL	VSS	2	254	254	10000	10000
Topology Guidelines							
Platform resistors values	Rpu=1KΩ, Rs=500Ω, Ri+Ragent=75-200Ω, R6+Rinvod=75-200Ω						
Platform resistors tolerances	± 5%						

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Title: *(Reserved)*

Size: A2 | Document Number: *RogueOne 13"* | Rev: *A00*

Date: Thursday, December 27, 2018 | Sheet 3 of 106

Main FUNC = CPU

HDMI 1.4B

57 HDMI_DDI_TX_N0
57 HDMI_DDI_TX_P0
57 HDMI_DDI_TX_N1
57 HDMI_DDI_TX_P1
57 HDMI_DDI_TX_N2
57 HDMI_DDI_TX_P2
57 HDMI_DDI_TX_N3
57 HDMI_DDI_TX_P3
57,89 CPU_DP1_CTRL_CLK
57 CPU_DP1_CTRL_DATA
57 CPU_DP1_HPD

TO DP MUX

58 DP2_DDI_TX_N0
58 DP2_DDI_TX_P0
58 DP2_DDI_TX_N1
58 DP2_DDI_TX_P1
58 DP2_DDI_TX_N2
58 DP2_DDI_TX_P2
58 DP2_DDI_TX_N3
58 DP2_DDI_TX_P3
58 DP2_AUX_CPU_P
58 DP2_AUX_CPU_N
58 DP2_HPD_CPU

EDP

55 eDP_TX_CPU_N0
55 eDP_TX_CPU_P0
55 eDP_TX_CPU_N1
55 eDP_TX_CPU_P1
55 eDP_AUX_CPU_N
55 eDP_AUX_CPU_P
55 EDP_HPD
24 L_BKLT_EN
55 L_BKLT_CTRL
55 EDP_VDD_EN
61 CNVI_EN#
89 eDP_RCOMP_CPU

3D3V_S0
SRN2K2J-4-GP
CPU_DP1_CTRL_DATA
CPU_DP1_CTRL_CLK
CPU_DP2_CTRL_CLK
CPU_DP2_CTRL_DATA
RN401
SIO_EXT_SMI#
R407
10KR2J-3-GP
2018.06.29

5.2.7 Compensation Signal Routing Guidelines

Table 5-20. eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Max Length
eDP_RCOMP	5 mils	25 mils	24.9 Ω ±1%	500 mils

Note: Must maintain low DC resistance routing (<5.1Ω)

5.2.8 eDP* Disabling and Termination Guidelines

Table 5-21. eDP* Disabling and Termination Guidelines

Pin name	Recommendation
eDP_TXN/P[3:0]	No connect
EDP_AUXN/P	No connect
GPP_E17/EDP_HPD/DISP_MISC4	Pull down to ground via 100k ohm resistor
DISP_RCOMP	Pull up to VCCIO via 100 ohm resistor
DISP_UTILS	No connect

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k ±5% resistor	NC

Table 9-1. Pin Straps (Sheet 3 of 4)

#566439

Signal	Usage	When Sampled	Comment
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E19 / DDPB_CTRLDATA / CNV_BT_IF_SELECT	Display Port B Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down . 0 = Port B is not detected. (Default) 1 = Port B is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E21 / DDPC_CTRLDATA	Display Port C Detected	Rising edge of PCH_PWROK	This signal has a weak internal Pull-down. 0 = Port C is not detected. (Default) 1 = Port C is detected. ***Notes:*** 1. The internal Pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_E23 / DDPD_CTRLDATA	Display Port D Detected	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = Port D is not detected. (Default) 1 = Port D is detected. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H17	Reserved	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.
GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

HDMI 1.4B

TO DP MUX

CPU1A
1 OF 20
HDMI_DDI_TX_N0 AL5
HDMI_DDI_TX_P0 AL6
HDMI_DDI_TX_N1 AJ5
HDMI_DDI_TX_P1 AJ6
HDMI_DDI_TX_N2 AF6
HDMI_DDI_TX_P2 AF5
HDMI_DDI_TX_N3 AE5
HDMI_DDI_TX_P3 AE6
DP2_DDI_TX_N0 AC4
DP2_DDI_TX_P0 AC3
DP2_DDI_TX_N1 AC1
DP2_DDI_TX_P1 AC2
DP2_DDI_TX_N2 AE4
DP2_DDI_TX_P2 AE3
DP2_DDI_TX_N3 AE1
DP2_DDI_TX_P3 AE2
DDI1_TXN0
DDI1_TXP0
DDI1_TXN1
DDI1_TXP1
DDI1_TXN2
DDI1_TXP2
DDI1_TXN3
DDI1_TXP3
DDI2_TXN0
DDI2_TXP0
DDI2_TXN1
DDI2_TXP1
DDI2_TXN2
DDI2_TXP2
DDI2_TXN3
DDI2_TXP3
Port B
Port C
Port A
EDP_TXN0 AG4
EDP_TXP0 AG3
EDP_TXN1 AG2
EDP_TXP1 AG1
EDP_TXN2 AJ4
EDP_TXP2 AJ3
EDP_TXN3 AJ2
EDP_TXP3 AJ1
EDP_AUX_N AH4
EDP_AUX_P AH3
DISP_UTILS AM7
DDI1_AUX_N AC7
DDI1_AUX_P AC6
DDI2_AUX_N AD4
DDI2_AUX_P AD3
DDI3_AUX_N AG7
DDI3_AUX_P AG6
eDP_TX_CPU_N0
eDP_TX_CPU_P0
eDP_TX_CPU_N1
eDP_TX_CPU_P1
eDP_AUX_CPU_N
eDP_AUX_CPU_P
DP2_AUX_CPU_N
DP2_AUX_CPU_P
DP Demux
GPP_E13/DDPB_HPD0/DISP_MISC0 CN6
GPP_E14/DDPC_HPD1/DISP_MISC1 CM6
GPP_E15/DDPD_HPD2/DISP_MISC2 CP7
GPP_E16/DDPE_HPD3/DISP_MISC3 CP6
GPP_E17/EDP_HPD/DISP_MISC4 CM7
CPU_DP1_HPD
CPU_DP2_HPD
SIO_EXT_SMI#
EDP_HPD
EDP_BKLTEN CK11
EDP_VDDEN CG11
EDP_BKLTCTL CH11
L_BKLT_EN
EDP_VDD_EN
L_BKLT_CTRL

1V_VCCIO
R401 1
24D9R2F-L-GP
2018.03.31 BOM option
R401
CNL:100 Ohm (64.10005.6DL)
WHL:24.9 Ohm (64.24R95.6DL)
Do Not Stuff
TP402
eDP_RCOMP_CPU AM6
DISP_RCOMP
CPU_DP1_CTRL_CLK CC8
CPU_DP1_CTRL_DATA CC9
CPU_DP2_CTRL_CLK CH4
CPU_DP2_CTRL_DATA CH3
GPP_E23_STRAP CP4
CNVI_EN# CR6
GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA
GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA
GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA
GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA
WHISKEY-LAKE-GP
ZZ.00CPU.271

Pin Straps (Sheet 4 of 4)

#566439

Signal	Usage	When Sampled	Comment
INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

RTC Gen 9 reset circuit_20170814
CPU_DP2_HPD
R404 1
Do Not Stuff
DP2_HPD_CPU
NON_RTC_RST
R403
100KR2J-1-GP
DP for Type-C Mux

Add RTC Gen 9 reset circuit_20170814 leakage issue
3D3V_S5_PCH
RTC_RST
R406
10KR2J-3-GP
RTC_RST
3D3V_S5_PCH
RTC_RST
R405
10KR2J-3-GP
Q401
CPU_DP2_HPD
DP2_HPD_CPU
3D3V_S5_PCH_R
2N7002KDW-1-GP
75.27002.F7C
RTC_RST

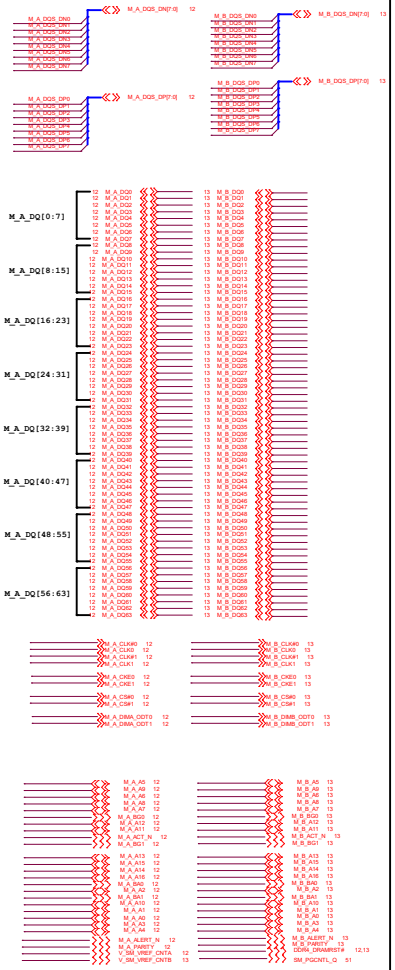
BOLT L 0823

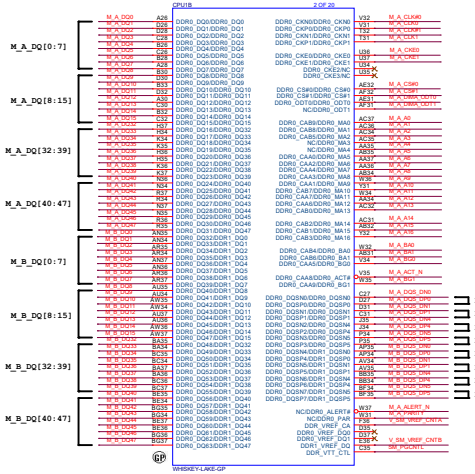
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

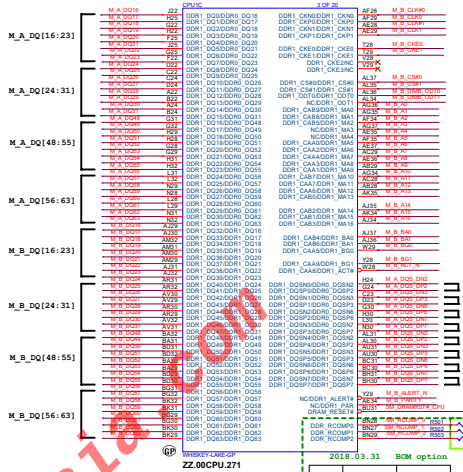
Title: CPU_(JTAG/CPU SIDE BAND)
Size: Custom | Document Number: RogueOne 13" | Rev: A00
Date: Thursday, December 27, 2018 | Sheet 4 of 106

Main FUNC = CPU

DDR4 ball type: Non-Interleaved Type







CPU TYPE	CNL	WHL
RS01	100 Ohm 64.10005.6DL	121 Ohm 64.12105.6DL
RS02	100 Ohm 64.10005.6DL	80.6 Ohm 64.80R65.6DL

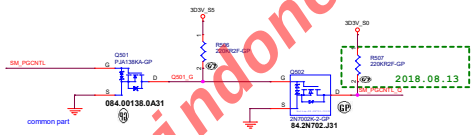
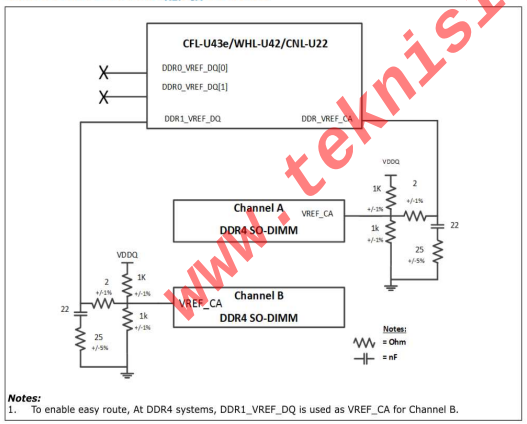
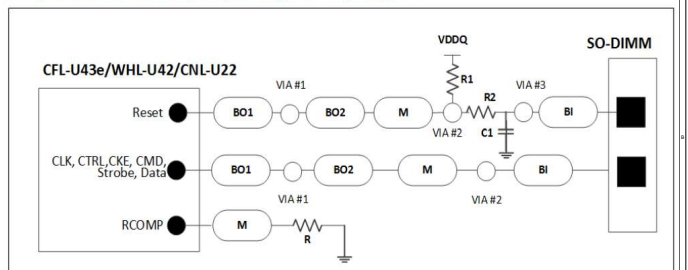


Figure 4-1. WHL U DDR4 SODIMM V_{REF-CA} Overview



Notes:
1. To enable easy route, At DDR4 systems, DDR1_VREF_DQ is used as VREF_CA for Channel B.

WHL U DDR4 SODIMM T3/8L Signals Topologies



Note: DRAM_RST C1 capacitor should not be installed

RCOMP (0/1/2)	M	US/SL	500				15	20	25	CFL-U43e/ WHL-U42: 121/80.6/ 100 CNL-U22: 100/100/ 100
Reset	BO1	US	500	8000			3		6	R1=470 [5%] R2=0 C1=0.1uF (no stuff)
	BO2	SL	800-BO1				3.5		12	
	M	SL			50		4		20	
	BI	US					4		20	

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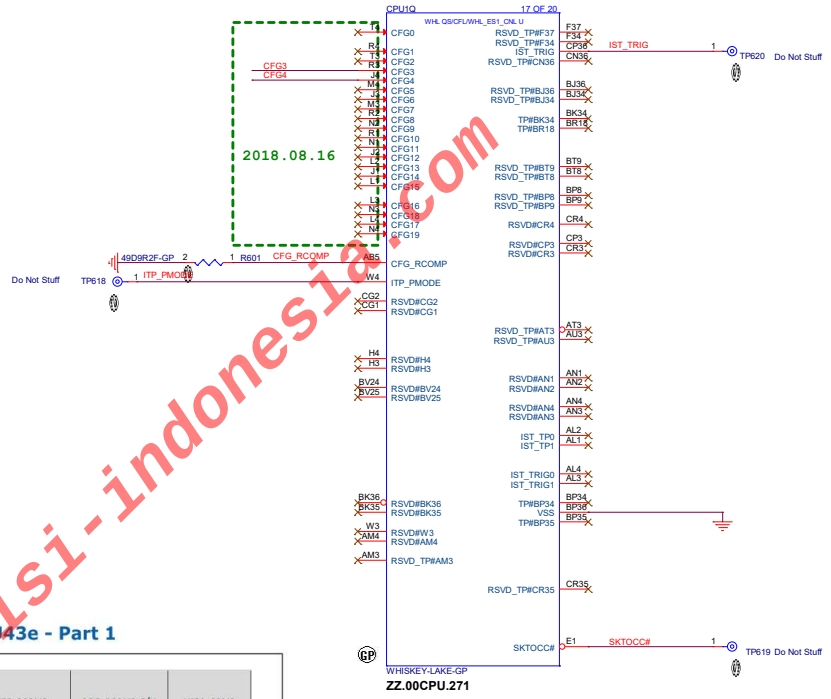
Title: CPU (DDR)

Size	Document Number	Rev
Custom	RogueOne 13"	A00

Date: Thursday, December 27, 2018 Sheet 5 of 105

Main FUNC = CPU

15 CFG3
15 CFG4



ZZ.00CPU.271

Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DDR4 SODIMM DDR_RCOMP	DSP_RCOMP	CFG_RCOMP	PCIE_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS DDR_RCOMP[2]: 162Ω ± 1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS DDR_RCOMP[2]: 100Ω ± 1% on pkg to VSS	24.9Ω +/-1% to VCCIO	49.9Ω +/-1% to GND	100Ω +/-1% Differential	113Ω +/-1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(RESERVED)

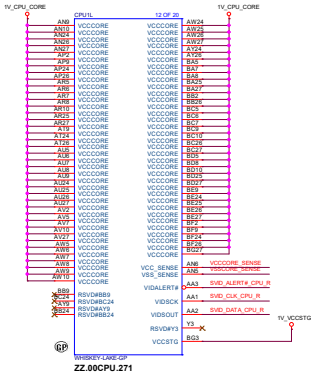
Size	Document Number	Rev
A2	RogueOne 13"	A00

Date: Thursday, December 27, 2018 Sheet 6 of 106

Main FUNC = CPU

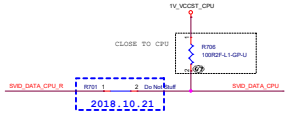
46 VCCCORE_SENSE
46 VSSCORE_SENSE

46 SVID_DATA_CPU
46 SVID_CLK_CPU
46 SVID_ALERT#_CPU

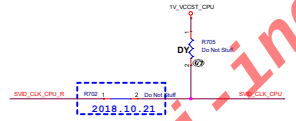


ZZ.00CPU.271

Layout Note:
The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
Route the Alert signal between the Clock and the Data signals.



SVID DATA



SVID CLOCK

SVID ALERT

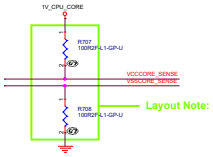


Figure 7-19. Routing Illustration for SVID Topology

#575412

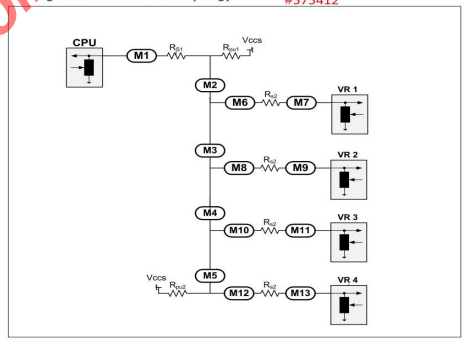
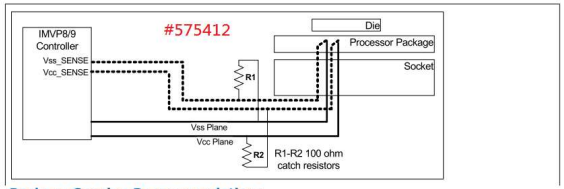


Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

SVID Signals	VIDSOUT, VIDSCK, VIDSALERT#
VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω
Platform resistors tolerances	± 5%
Route ordering	When routing at minimum spacing route Alert between Data and Clock

12-3. Example of Processor Vcc_SENSE/Vss_SENSE Package Sensing



Package Sensing Recommendations

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
	100Ω	50Ω	<25 mils
Vcc_SENSE /Vss_SENSE			
Vcc_{GT}_SENSE / Vss_{GT}_SENSE			
Vcc_{SA}_SENSE / Vss_{SA}_SENSE			
Vcc_{IO}_SENSE / Vss_{IO}_SENSE[1]		NA	

Note:
1. Does not apply when rails are merged.

To minimize any stray noise pickup to the Vcc_SENSE/ Vss_SENSE lines

- Sense traces should be referenced to a solid ground plane
- Avoid crossing over plane splits
- Maintain 25-mil separation distance away from any other dynamic signals

— R1, R2 should be placed within 2 inches (50.8 mm) of the processor socket, minimizing any potential error due to Vcc_SENSE/Vss_SENSE line resistance.

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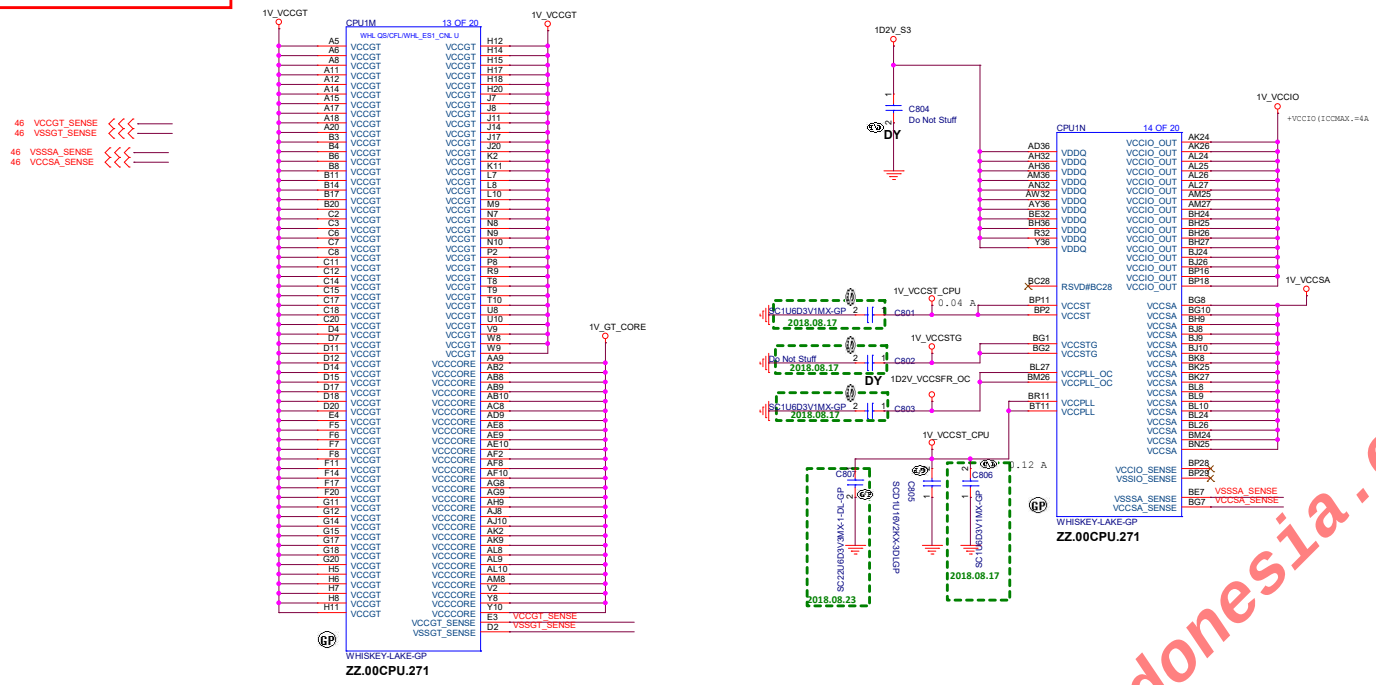
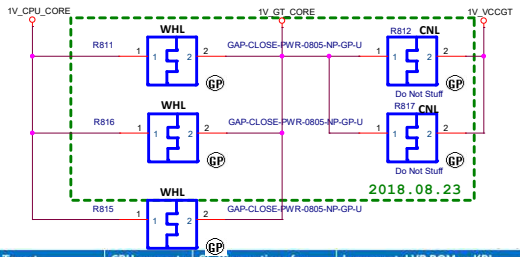
File:
CPU(VCC_CORE)

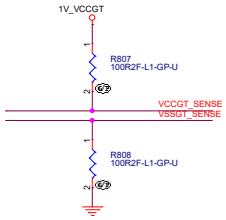
Size	Document Number	Rev
A3	RogueOne 13"	A00

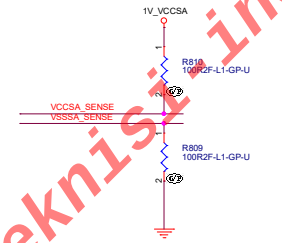
Date: Thursday, December 27, 2018 Sheet 7 of 86

Main FUNC = CPU









Design Target	CPU support	Stuffing options for compatibility	Incremental VR BOM vs KBL	Incremental board area vs. KBL
Cost optimized entry design (Ci3 SM80-ICP)	CNL only	None	No increase expected for CNL vs. KBL U22	~0mm² vs. KBL U22
Premium design (Ci7-Ci3)	WHL only	None	Load line change anticipated to drive incremental cost vs. KBL R	TBD
Scalable mainstream design (Ci7-ICP)	WHL and CNL	Jumpers vary by SKU: 3 if WHL 1 if CNL	Load line change on WHL anticipated to drive incremental cost vs. KBL R No increase expected for CNL vs. KBL U22	TBD

Pin Number	CFL-U43E	WHL ES1 Netname	WHL ES2 Netname
AA9	VCCGT	VCCGT	VCCCORE
AB10	VCCGT	VCCGT	VCCCORE
AB2	VCCGT	VCCGT	VCCCORE
AB8	VCCGT	VCCGT	VCCCORE
AB9	VCCGT	VCCGT	VCCCORE
AC8	VCCGT	VCCGT	VCCCORE
AD9	VCCGT	VCCGT	VCCCORE
AE10	VCCGT	VCCGT	VCCCORE
AE8	VCCGT	VCCGT	VCCCORE
AE9	VCCGT	VCCGT	VCCCORE
AF10	VCCGT	VCCGT	VCCCORE
AF2	VCCGT	VCCGT	VCCCORE
AF8	VCCGT	VCCGT	VCCCORE
AG8	VCCGT	VCCGT	VCCCORE
AG9	VCCGT	VCCGT	VCCCORE
AH9	VCCGT	VCCGT	VCCCORE
AJ10	VCCGT	VCCGT	VCCCORE
AJ8	VCCGT	VCCGT	VCCCORE
AK2	VCCGT	VCCGT	VCCCORE
AK9	VCCGT	VCCGT	VCCCORE
AL10	VCCGT	VCCGT	VCCCORE
AL8	VCCGT	VCCGT	VCCCORE
AL9	VCCGT	VCCGT	VCCCORE
AM8	VCCGT	VCCGT	VCCCORE
V2	VCCGT	VCCGT	VCCCORE
Y10	VCCGT	VCCGT	VCCCORE
Y8	VCCGT	VCCGT	VCCCORE

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Title: CPU_(DISPLAY)

Size: A2 | Document Number: RogueOne 13" | Rev: A00

Date: Thursday, December 27, 2018 | Sheet 8 of 106

Main Func = CPU

(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *(Reserved)*

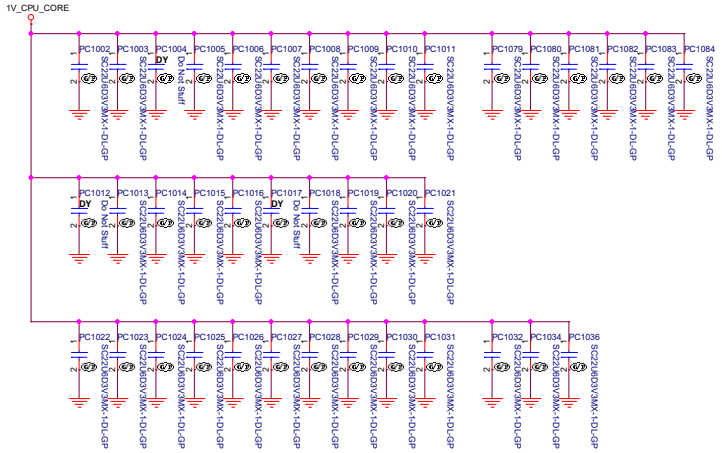
Size	Document Number	Rev
A3	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 9 of 106

Main FUNC = CPU

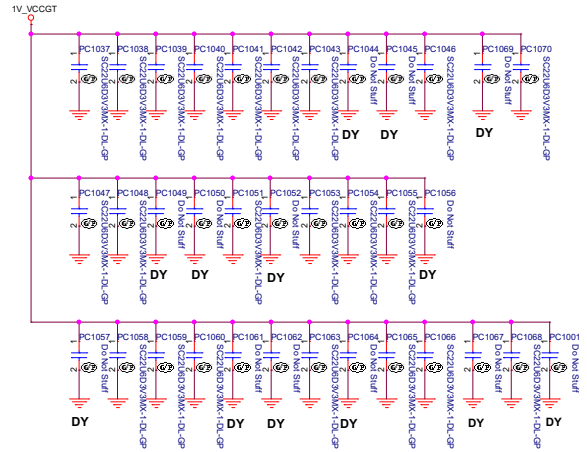
1V_CPU_CORE

22U 0603 x 39 (3DY)



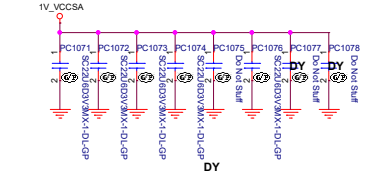
VCCGT

22U 0603 x 35 (3 DY)



VCCSA

22U 0603 x 8 (3DY)



KBL-R U42 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
Vcc Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
	1x 220 uF (@4.5mO ESR)	Placed at backside side near to VR output
Vcc_{GT} Power Plane at VR output	2x 220 uF (@4.5mO ESR)	Placed at primary side near to VR output
V_{DDQ} Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
Vcc_{IO} Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
Vcc_{SA} Power Plane at VR output	2x 47 uF 0805	Placed at primary side near to VR output
Vcc_{PLL} Power Plane at V1P0A VR output	1x 0.1uF 0402	Placed at primary side near to VR output

Notes:
1. These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
2. Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

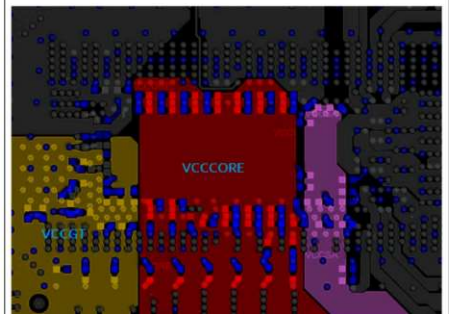
KBL-R U42 Decoupling Requirements (Sheet 1of 2)

Domain	Backside cap	Primary side cap	Placement guideline
Vcc	7x 10 uF 0402		Place on secondary side, underneath the package
	26x 1 uF 0402 or 0201		Refer to diagram in Note 3 below for placement recommendation of 0201 caps
		9x 22 uF 0603	Place as close to the package as possible
		8x 47 uF 0805 (6.3V)[1]	
Vcc_{GT}	12x 10 uF 0402		Place on secondary side, underneath the package
	14x 1 uF 0402 or 0201		
		7x 22 uF 0603	Place as close to the package as possible
		3x 47 uF 0805 (6.3V)[1]	
Vcc_{SA}	7x 10 uF 0402		Place on secondary side, underneath the package
	7x 1 uF 0402 or 0201		
		6x 10 uF 0402	Place as close to the package as possible
Vcc_{IO}		4x 1 uF 0402	Place as close to the package as possible
V_{DDQ}		4x 10 uF 0402	Place as close to the package as possible
		3 x 22 uF 0603	Place as close to the package as possible
V_{DDQC}		1 x 10 uF 0402	Preferred to place the 0402 10uF cap on the secondary under the package shadow near VDDQC pin and short to VDDQ rail under with a shape. Alternatively, if the 0402 cap cannot be placed on the backside, follow the example showed in Figure 48-3. The 0402 cap to VDDQC BGA routing should not exceed 48mohm (Rdc). RVP design uses trace L=450mil, W=8mil between BGA and cap. Additional trace routing implemented in RVP design was not required.
Vcc_{PLL}		1x 1 uF 0402	Place as close to the package as possible.
Vcc_{PLL_OC}		1x 1 uF 0201	Do not route Vcc_{PLL}, Vcc_{PLL_OC}, Vcc_{ST} closest adjacent layer over any power net other than ground.
Vcc_{ST}		1x 1 uF 0402	For VccST: Refer to Figure 48-2 for additional routing details for VccST & VccSTG.

KBL-R U42 Decoupling Requirements (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline

Notes:
1. The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR
2. Component placement order: Package edge > 0402 caps > 0805 caps > Bulk caps >Power source
3. Diagram of placement for 0201 or 0402 backside caps for CPU decoupling.



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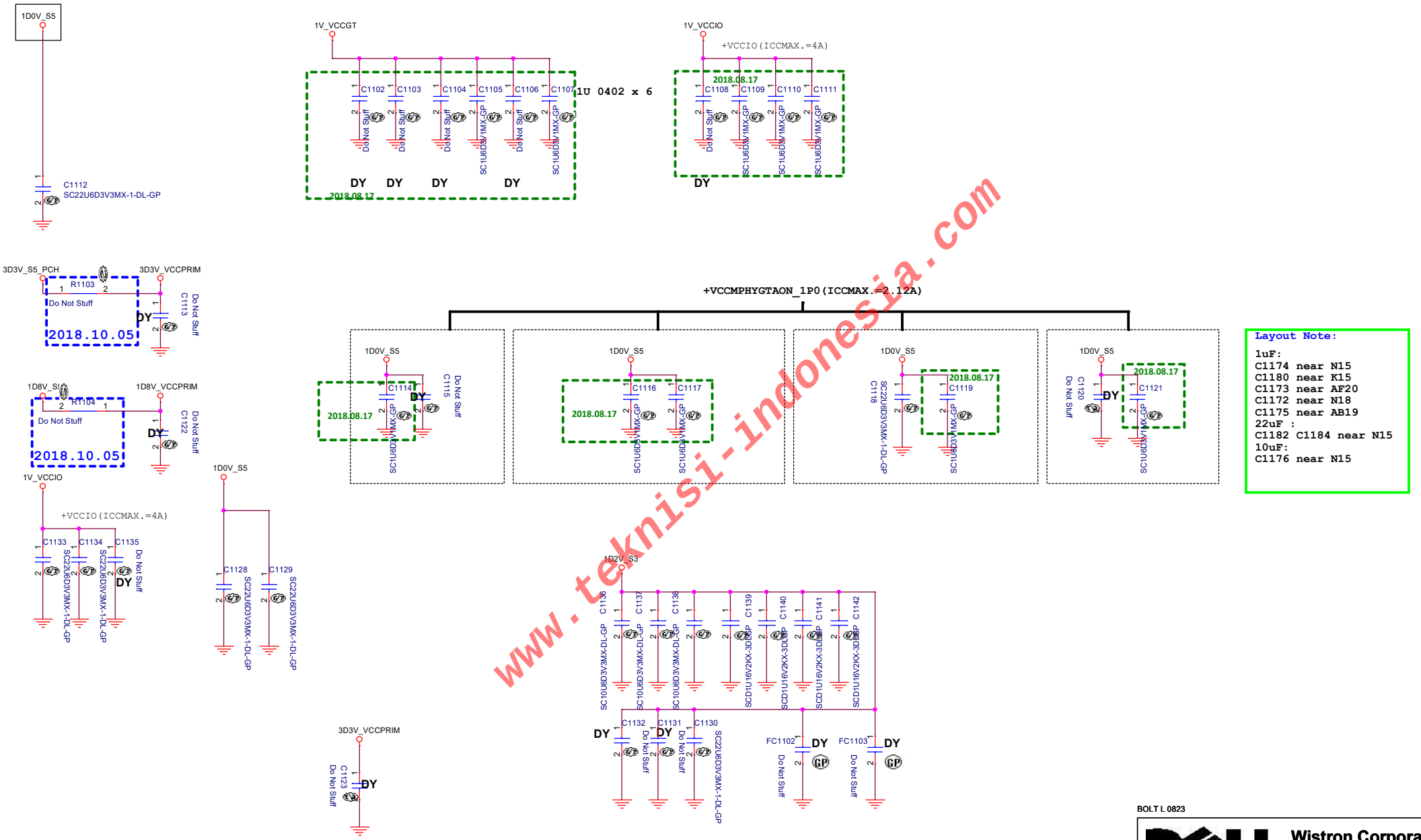
Title: CPU_(Power CAP1)

Size: A2 | Document Number: RogueOne 13" | Rev: A00

Date: Thursday, December 27, 2018 | Sheet 10 of 106

Main FUNC = CPU

PCH DERIVED RAILS UNSLICED GT VCCIO



Layout Note:

1uF:
C1174 near N15
C1180 near K15
C1173 near AF20
C1172 near N18
C1175 near AB19
22uF :
C1182 C1184 near N15
10uF:
C1176 near N15

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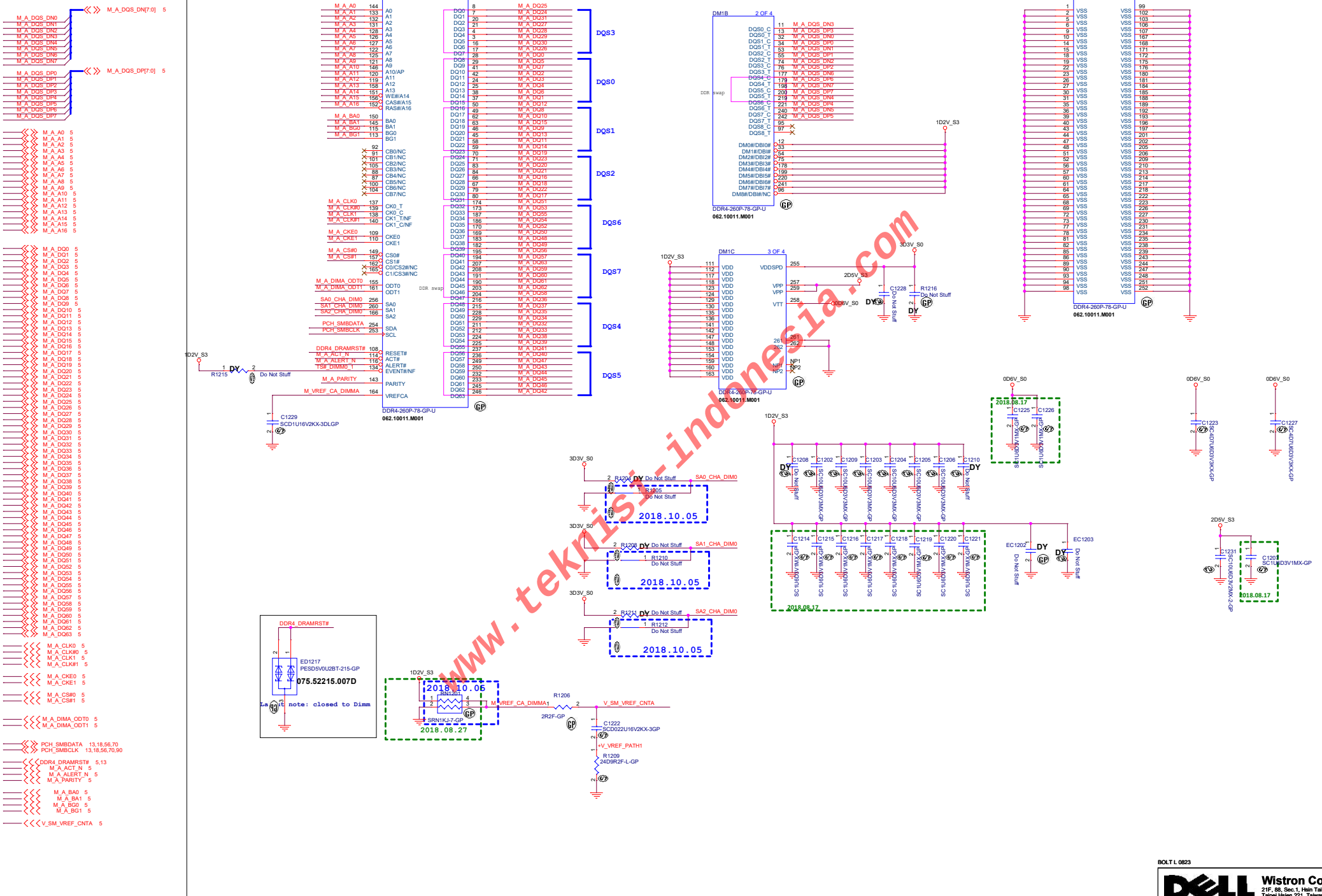
Title	CPU_(Power CAP2)	
Size A3	Document Number RogueOne 13"	Rev A00
Date: Thursday, December 27, 2018	Sheet 11 of 106	

Main Func = MEMORY



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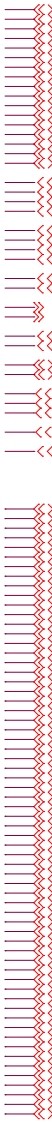
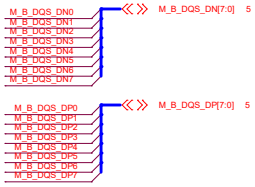
Title: DDR3-SODIMM1

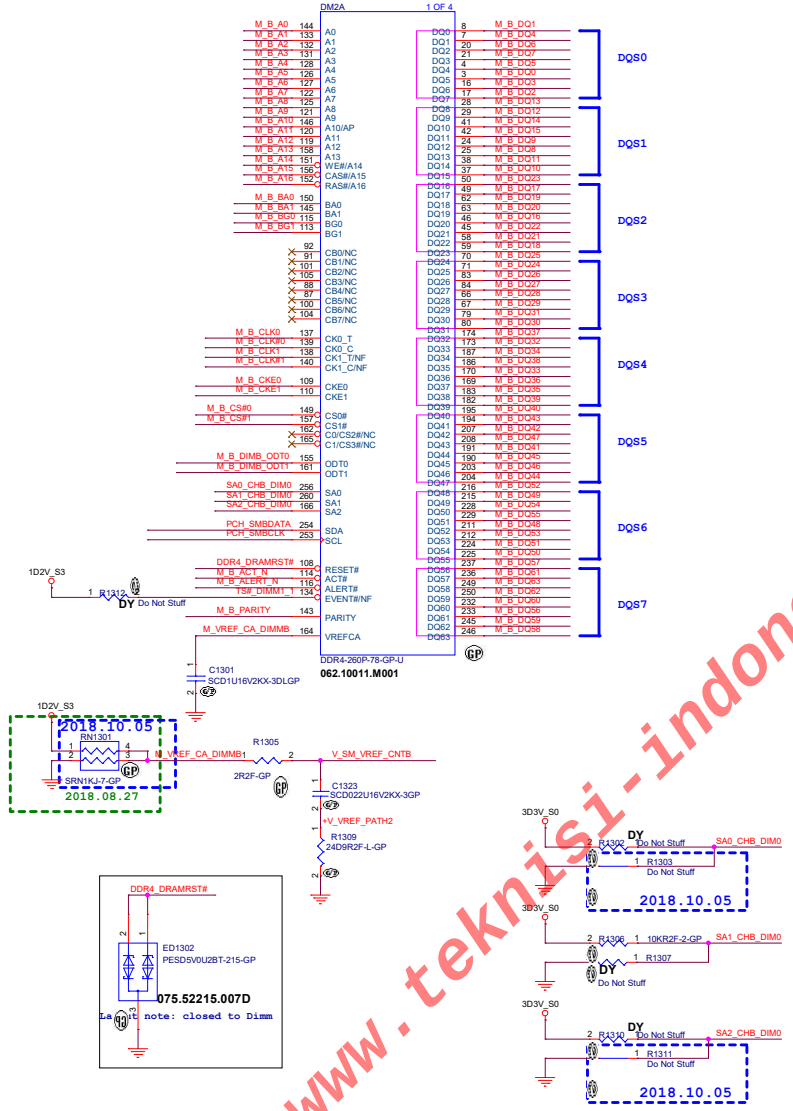
Size: A2 | Document Number: BOLT WHL | Rev: A00

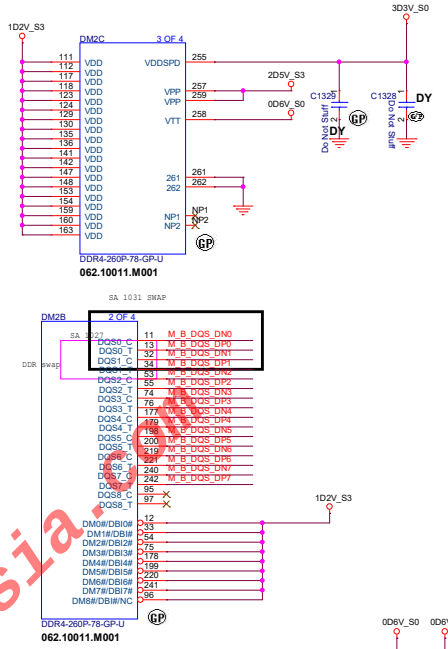
Date: Thursday, December 27, 2018 | Sheet 12 of 106

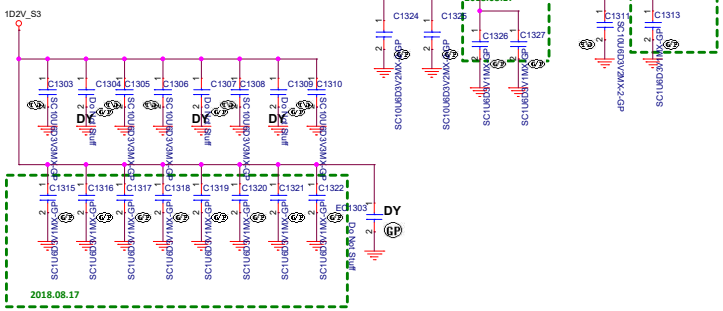
Main Func
= MEMORY











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Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM1

Size	Document Number	Rev
A2	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 13 of 106

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Taipei Hsien 221, Taiwan, R.O.C.

Title
(Reserved)_SODIMM _SODIMM4

Size	Document Number	Rev
A4	BOLT WHL	*A00*

Date: Thursday, December 27, 2018 Sheet 14 of 106

Main Func = PCH

GPP_B18 / GSPI0_MOSI	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. (Default) 1 = **Enable** "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

GPP_B18

GPP_C2 / SMBALERT#	TLS Confi-dentiality	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **Disable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default) 1 = **Enable** Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_C2

GPP_C5 / SMLOALERT#	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = **LPC** is selected (for EC). (Default) 1 = **eSPI** is selected (for EC). ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **If this strap is configured to '0' (eSPI is disabled), the *eSPI Flash Sharing Mode* strap must be configured to '0' as well (SAFS is disabled)**

GPP_C5

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_MOSI

GPP_D12 / ISH_SPI_MOSI / GSPI2_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

GPP_D12

SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO2

SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SPI0_IO3

HDA_SDO / I2S0_TXD	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. (Default) 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external Pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PCH_PWROK is high. 2. This signal is in the primary well.

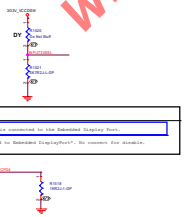
GPP_H21	XTAL Frequency Select	Rising edge of RSMRST#	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.

GPP_H21

GPP_F6 / CNV_RGI_DT	M.2 CNV Mode Select	Rising edge of RSMRST#	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

PCH strap pin:

INPUT3VSEL	3.0V Select	Input pin must always be driven to a valid logic level	External pull-up or pull-down is required 0 = 3.3V supply is 3.3V +/- 5% 1 = 3.3V supply is 3.0V +/- 5% ***Note:*** This strap should only be used for specific targeted 1S battery systems.



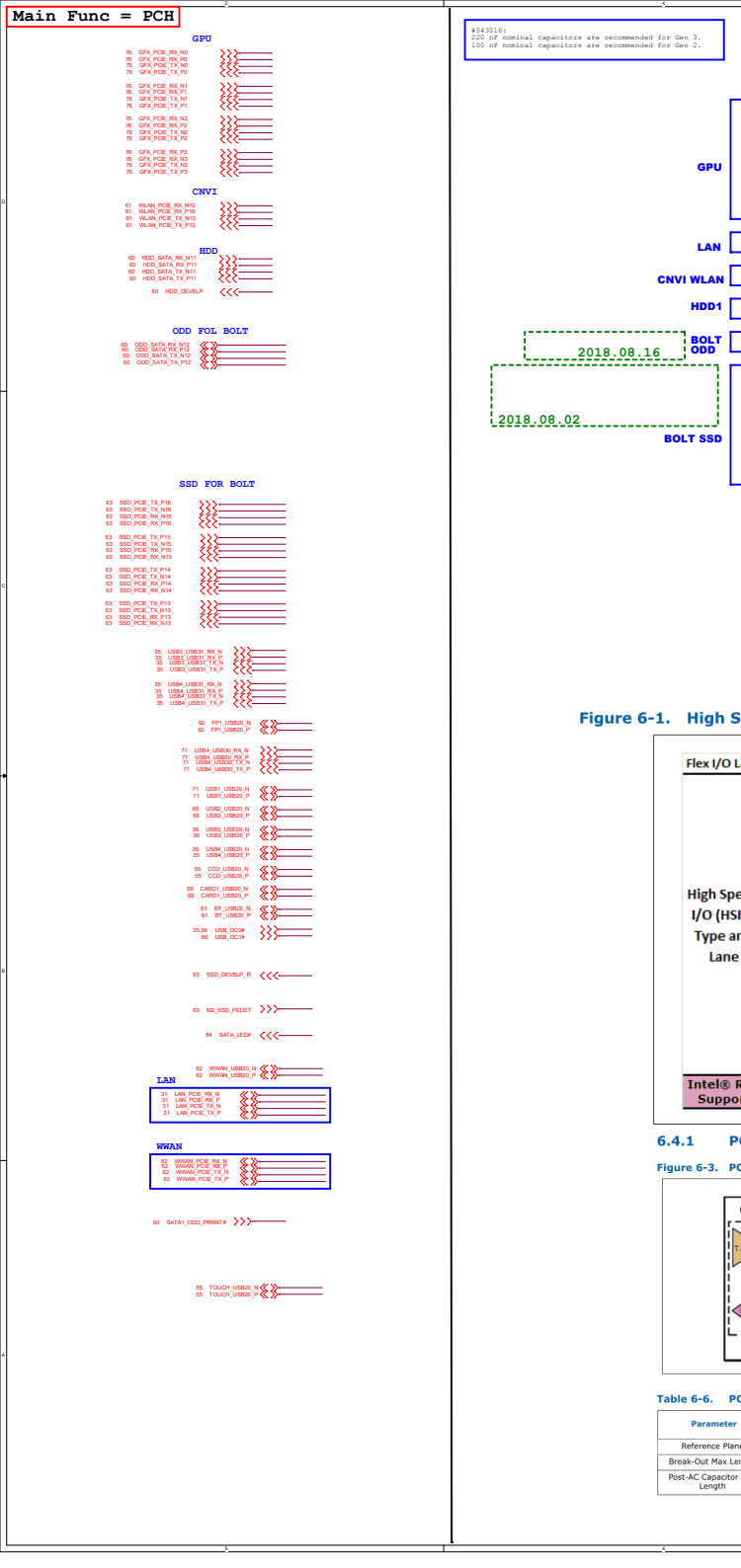
GPD7	Reserved	Rising edge of DSW_PWROK	External pull-up is required. Recommend 100K. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling

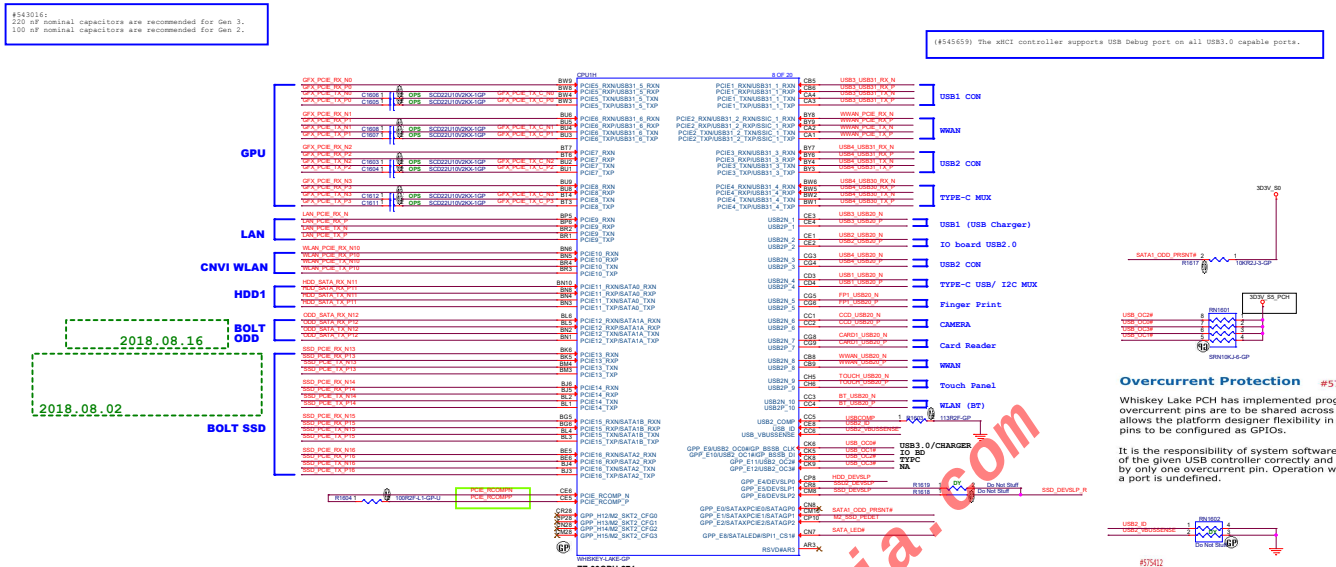
GPP_H23	eSPI Flash Sharing Mode	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Master Attached Flash Sharing (MAFS) enabled (Default) 1 = Slave Attached Flash Sharing (SAFS) enabled. ***Notes:*** 1. The internal pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well. ***Warning:*** **This strap must be configured to '0' (SAFS is disabled) if the *eSPI or LPC* strap is configured to '0' (eSPI is disabled)**

Wistron Corporation

CPU (CS-24EMMC)

RogueOne 13"





USB 2.0 Table

Pair	Device
1	USB1 (USB Charger)
2	IO board USB2.0
3	USB2 CON
4	TYPE-C USB/ I2C MUX
5	Finger Print
6	CAMERA
7	Card Reader
8	WWAN
9	Touch Panel
10	WLAN (BT)

Overcurrent Protection #575412

Whiskey Lake PCH has implemented programmable USB Overcurrent signals. The 4 overcurrent pins are to be shared across the USB 2.0 ports and USB 3.1 ports. This allows the platform designer flexibility in routing of the OC pins and allows for unused pins to be configured as GPIOs.

It is the responsibility of system software (BIOS) to program the overcurrent registers of the given USB controller correctly and to make sure that each USB port is protected by only one overcurrent pin. Operation with more than one overcurrent pin mapped to a port is undefined.

#575412

USB_ID and VBUS_SENSE signals are not needed for USB Type-C implementation with Type-C Port Controller (TCPC).

Figure 6-1. High Speed I/O (HSIO) Lane Multiplexing in CNL PCH-LP

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	GbE	GbE	GbE		SATA 0	SATA 1a	GbE	GbE	SATA 1b	SATA 2
Intel® RST Support	No Support				No Support				Yes				Yes			

Figure 3-1. RCOMP Recommendation for WHL U42 and CFL U43e - Part 1

	LP3 DDR_RCOMP	DDR4 SODIMM DDR_RCOMP	DISP_RCOMP	CFG_RCOMP	PCIE_RCOMP_P/N	USB2_COMP
Board Rterm (ohm)	DDR_RCOMP[0]: 200Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS DDR_RCOMP[2]: 162Ω ± 1% on pkg to VSS	DDR_RCOMP[0]: 121Ω ±1% on pkg to VSS DDR_RCOMP[1]: 80.6Ω ± 1% on pkg to VSS DDR_RCOMP[2]: 100Ω ± 1% on pkg to VSS	24.9Ω +/-1% to VCCIO	49.9Ω +/-1% to GND	100Ω +/-1% Differential	113Ω +/-1% to GND
Board Rdc (ohm)	n/a	n/a	<0.2	<0.5	<0.1	<0.5
DDR	X	X				
HDMI			X			
DP			X			
eDP			X			
CFG				X		
PCIe					X	
USB2						X

6.4.1 PCH PCI Express* Device Down Guidelines

Figure 6-3. PCH PCI Express* Device Down at 2.5, 5, and 8 GT/s Topology

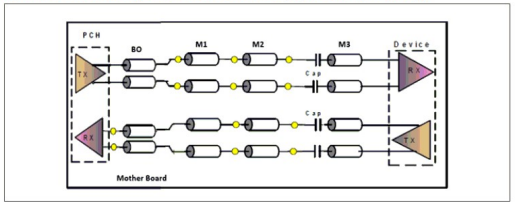


Table 6-6. PCH PCI Express* Device Down Routing Guidelines (Sheet 1 of 2)

Parameter	Segment	Stack-up (MS/SL/DSL)	Units	2.5 GT/s Routing	5GT/s Routing	8 GT/s Routing
Reference Plane	BO, M1, M2, M3	MS/SL/DSL	NA	GND	GND	GND
Break-Out Max Length	BO	MS/SL/DSL	mm(mils)	15.2(598.42)	15.2(598.42)	15.2(598.42)
Post-AC Capacitor Max Length	M3	MS	mm(mils)	8(314.96)	8(314.96)	8(314.96)

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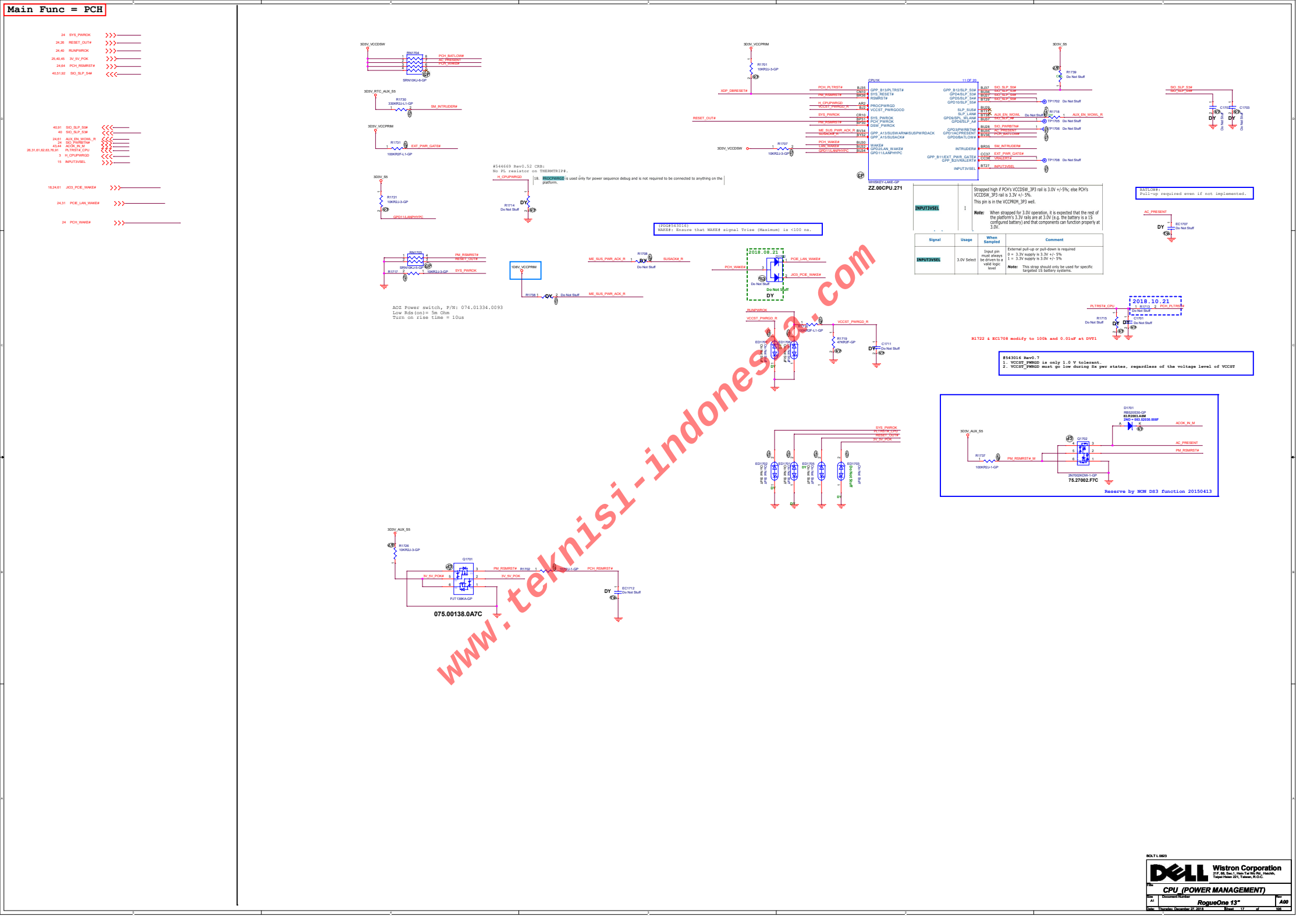
File: CPU (PCIE/SATA/USB)

Size: A1 | Document Number: BOLT WHL | Rev: A00

Date: Thursday, December 27, 2018 | Sheet 18 of 166

Main Func = PCH



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Wistron Corporation
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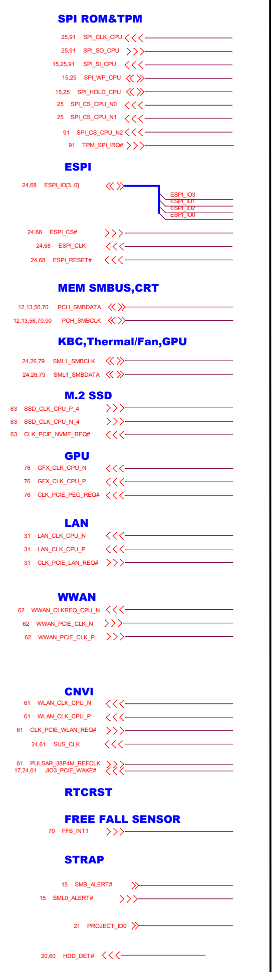
CPU (POWER MANAGEMENT)

Size: A1 | Document Number: RogueOne 13" | Rev: A00

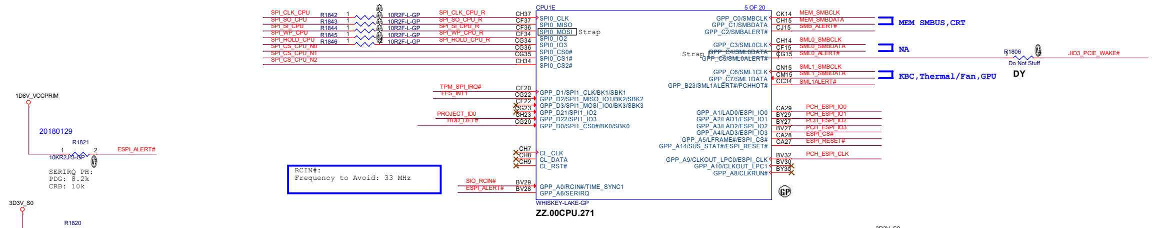
Date: Thursday, December 27, 2018 | Sheet 17 of 106

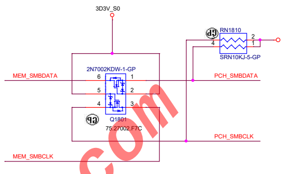
Main Func = PCH

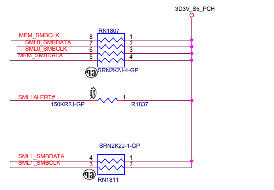


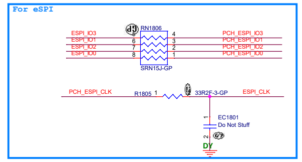
R1842/R1843/R1844/R1845/R1846

CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt-L(TPM)	64.10R05.6DL	63.5R134.1DL
Bolt (non TPM)	63.5R134.1DL	64.49R95.6DL









For eSPI

CPU_SMB_ALERT#_P0

Table 3: Platform Supported Pin Strap Settings for LPC / eSPI / SPI Flash

ESPI Enable Strap (ESPI_EN) Value (0: LPC, 1: eSPI)	Boot BIOS Strap (BBS) Value (0: SPI, 1: LPC/eSPI)	EC Connection	Boot (BIOS) Flash Connection (Section 3.1.4)
0	0	LPC	SPI
0	1	LPC	LPC
1	0	eSPI	SPI
1	1	eSPI	eSPI (to EC over eSPI Peripheral Channel) (refer to Section 3.1.4 for details)

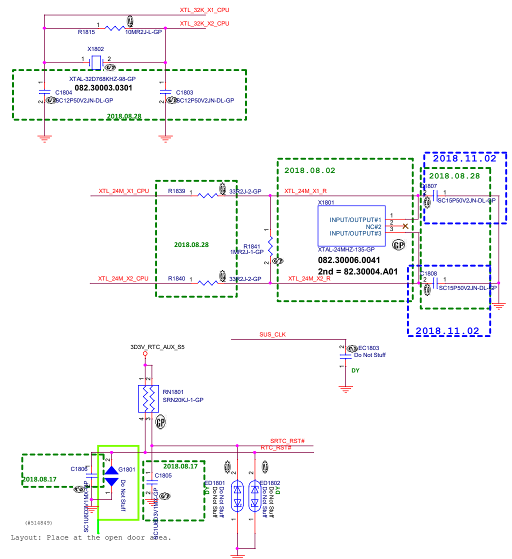
PCH strap pin:

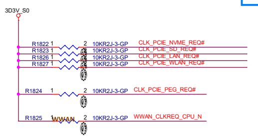
eSPI or LPC	Sampled at rising edge of RSMRST#
SML0ALERT# / GPP_C5	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. 1 = eSPI Is selected for EC.

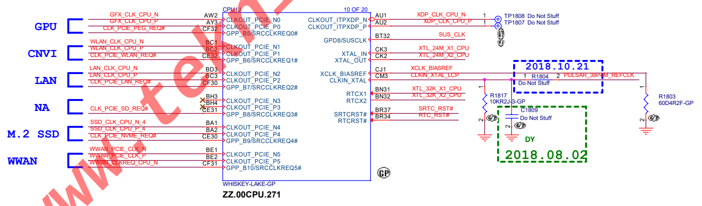
This signal has a weak internal pull-down.

Table 9-1. Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
GSPI1_MOSI/ GPP_B22	Boot BIOS Strap Bit BBS	Rising edge of PCH_PWROK	This Signal has a weak internal Pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6 / Boot BIOS Destination 0 / SPI (Default) 1 / LPC **Notes:** 1. The internal Pull-down is disabled after PLTRST# de-asserts. 2. If option 1 (LPC) is selected, BIOS may still be placed on LPC, but all platforms are required to have SPI flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot. 3. Boot BIOS Destination select to LPC by functional strap or using Boot BIOS Destination bit will not affect SPI accesses initiated by Intel ME or Integrated GbE LAN. 4. This signal is in the primary well.
SML0ALERT#/ GPP_C5	eSPI or LPC	Rising edge of RSMRST#	This signal has a weak internal Pull-down. 0 = **LPC** Is selected for EC. (Default) 1 = **eSPI** Is selected for EC. **Notes:** 1. The internal Pull-down is disabled after RSMRST# de-asserts. 2. This signal is in the primary well.







CLKIN_XTAL	I		XTAL Clock Input: Single ended integrated CNV (Connectivity) XTAL clock input

Group	Signal Name	Description
System Management	INTRUDER#	Intruder Detect: This signal can be set to disable system if box detected open.
RTC	SRTCRST#	Secondary RTC Reset: This signal resets the manageability register bits in the RTC well when the RTC battery is removed.
RTC	RTCRST#	RTC Reset: When asserted, this signal resets register bits in the RTC well.

Figure 7-11. XCLK Bias Reference Topology

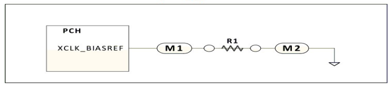


Table 7-8. XCLK Bias Reference Routing Guideline (Sheet 1 of 2)

Parameter	Segment	Stack-up	Rule
Reference Plane	M1, M2	MS/SL/DSL	Ground
Single Ended Trace Impedance	M1, M2	MS/SL/DSL	Refer Note
Max Total Length	M1+M2	MS/SL/DSL	1000mils(25.4mm)
Resistor (R1)			60 Ohm ±1.0%
Max Transition Via Count			2

Main Func = PCH

KB BL LED

65 KB_LED_BL_DET

EDP DMIC

55 DMIC_PCH_CLK

55 DMIC_PCH_DATA

CNVI

61 BT_PCMOUT_CLKREQ0

61 BT_PCMFRM_RSTN

CODEC

27 HDA_SYNC_CODEC

27 HDA_SDOUT_CODEC

27 HDA_BITCLK_CODEC

27 HDA_SDIN0_CPU

27 SPKR

DEBUG PORT

68 ME_FWP_R

STRAP

15 HDA_SDOUT_CPU

24 GC6_THM_DIS#_PCH

21,24,62 WWAN_DB_DET#

LAN CABLE

31 LOM_CABLE_DETECT#

24,85 DGPU_PWROK

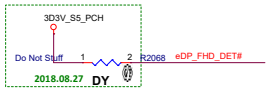
66 IO_DB_DET#_GPPG5

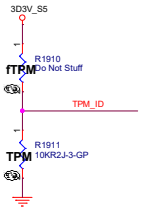
eDP_FHD_DET# 55

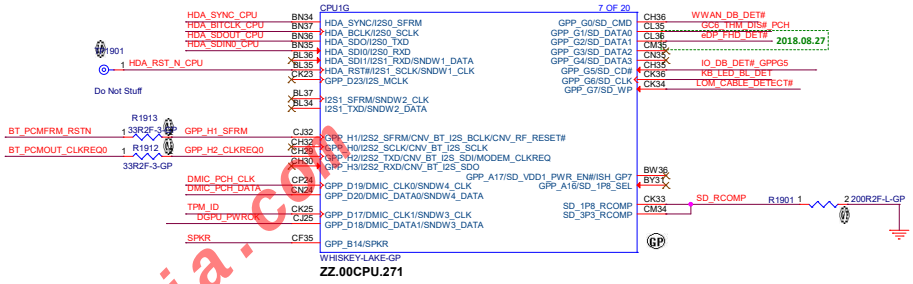
Strap pin:

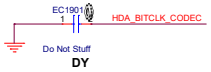
Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. * 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. * 1 = Port C is detected.

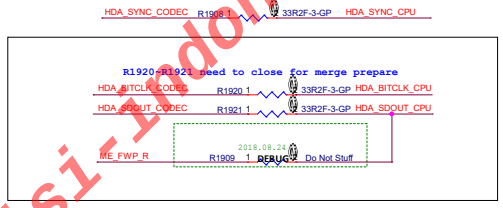
These two signals have weak internal pull-down.











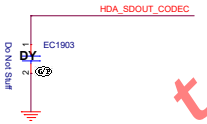


Figure 3-2. RCOMP Recommendation for WHL U42 and CFL U43e - Part 2

	SD_RCOMP_1P8	SD_RCOMP_3P3	EMMC_RCOMP	XCLK_BIASREF	CNV_WT_RCOMP	PCH_OPIRCOMP	PROC_POPIRCOMP
Board Rterm (ohm)	200Ω +/-1% to GND	200Ω +/-1% to GND	200Ω +/-1% to GND	60Ω +/-1% to GND	150Ω +/-1% to GND	49.9Ω +/-1% to GND	49.9Ω +/-1% to GND
	Notes: SD_RCOMP_1P8, SD_RCOMP_3P3 and EMMC_RCOMP can be merged into one 200Ω +/-1% to GND resistor. Routing each of them to individual 200Ω +/-1% to GND resistor is an option too.						
Board Rdc (ohm)	<0.1	<0.1	<0.1	<0.5	<0.5	<0.2	<0.2
SD3	X	X					
EMMC			X				
POPI						X	X
XTAL				X			
CNVi_DPHY					X		

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Title: CPU_(AUDIO/SDIO/SDXC)

Size: A2 | Document Number: RogueOne 13" | Rev: A00

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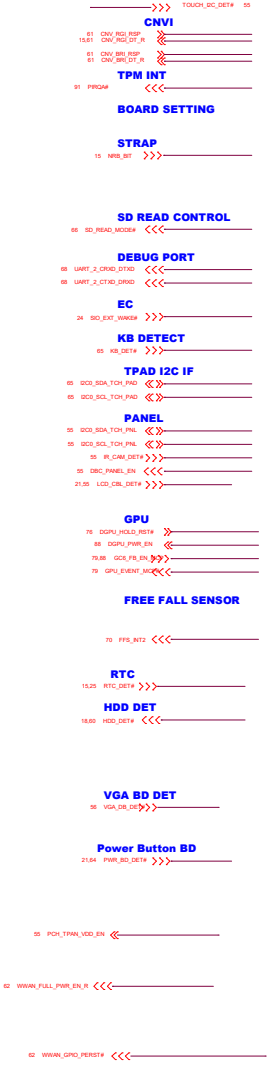
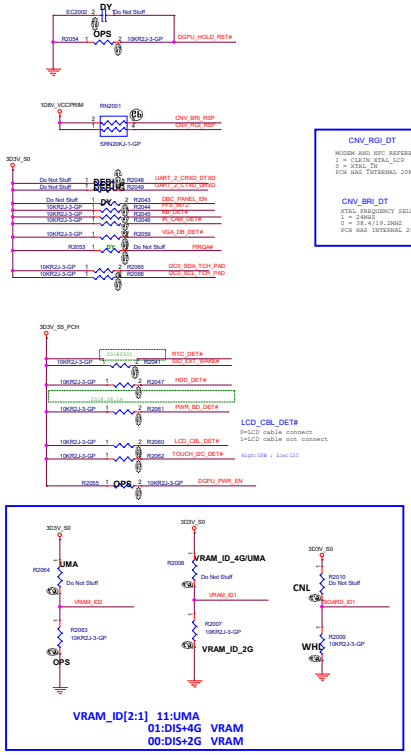
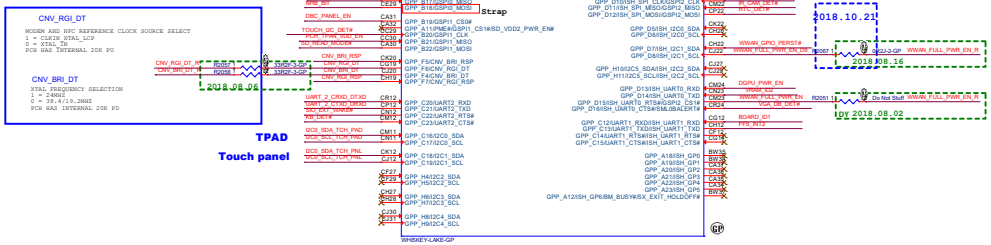
Main Func = PCH







17.4.1 Configurable GPIO Voltage

Except for all pads in GPIO F group and GPD group, all other GPIO pads support per-pad configurable voltage, which allows control selection of 1.8V or 3.3V for each pad. The configuration is done via soft straps.

Before soft straps are loaded, the default voltage of each pin depends on its default as input or output.

- Input: 1.8V level with 3.3V tolerant.
- Output: defaults to '0', except for the following GPIOs which defaults to '1' via a ~20K pull-up to 3.3V:
  - GPP_B0
  - GPP_B1
  - GPP_B11 / EXT_PWR_GATE#
  - GPP_B12 / SLP_S0#
  - GPP_H18 / CPU_C10_GATE#

A 1.8V device connected to these GPIOs must be capable of taking 20K pull-up to 3.3V.

'arning: GPIO pad voltage configuration must be set correctly depending on device connected to it; otherwise, damage to the PCH or the device may occur.

otes: - GPIO F group supports 1.8V only.

- GPD group supports 3.3V only.

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File:

CPU (LPSS/ISH)

Size	Document Number	Rev
A1	RogueOne 13"	A00

Date: Friday, December 28, 2018 Sheet 20 of 106

Main Func = CPU

61 BLUETOOTH_EN
61 WIFI_RF_EN

20,64 PWR_BD_DET#

15 GPP_H21
15 GPP_H23
15 GPD_7

40 GPPC_H18_VCCIO_LPM

18 PROJECT_ID0

CNvi TX for wifi

61 CNV_WT_CLK_DP
61 CNV_WT_CLK_DN
61 CNV_WT_DP0
61 CNV_WT_DN0
61 CNV_WT_DP1
61 CNV_WT_DN1

CNvi RX for wifi

61 CNV_WR_CLK_DP
61 CNV_WR_CLK_DN
61 CNV_WR_DP0
61 CNV_WR_DN0
61 CNV_WR_DP1
61 CNV_WR_DN1

LTE COEX

19,24,62 WWAN_DB_DET#

62 WWAN_BB_RST#

20,55 LCD_CBL_DET#

66 IO_DB_DET#

CPU1I — 9 OF 20 — WHISKEY-LAKE-GP

CNVI FOR WIFI

CNV_WR_DN0 CR30 — CNV_WR_D0N
CNV_WR_DP0 CP30 — CNV_WR_D0P
CNV_WR_DN1 CM30 — CNV_WR_D1N
CNV_WR_DP1 CN30 — CNV_WR_D1P
CNV_WT_DN0 CN32 — CNV_WT_D0N
CNV_WT_DP0 CM32 — CNV_WT_D0P
CNV_WT_DN1 CP33 — CNV_WT_D1N
CNV_WT_DP1 CN33 — CNV_WT_D1P
CNV_WR_CLK_DN CN31 — CNV_WR_CLKN
CNV_WR_CLK_DP CP31 — CNV_WR_CLKP
CNV_WT_CLK_DN CP34 — CNV_WT_CLKN
CNV_WT_CLK_DP CN34 — CNV_WT_CLKP

R2101 1 150R2F-1-GP — CNV_WT_RCOMP — CR32 — CNV_WT_RCOMP#CP32 / CNV_WT_RCOMP#CR32
2018.09.07
Do Not Stuff
TP2101
CNV_PA_BLANKING — CP20 — GPP_F0/CNV_PA_BLANKING
PROJECT_ID1 — CK19 — GPP_F1
PROJECT_ID2 — CG17 — GPP_F2
FOR DISCREATE COEX
PWR_BD_DET# — CR14
BLUETOOTH_EN — CP14 — GPP_C8/UART0_RXD
LCD_CBL_DET# — CN14 — GPP_C9/UART0_TXD
IO_DB_DET# — CM14 — GPP_C10/UART0_RTS# / GPP_C11/UART0_CTS#
2018.08.02
Do Not Stuff TP2102 — CNV_MFUART2_RXD — CH17 — GPP_F8/CNV_MFUART2_RXD
Do Not Stuff TP2103 — CNV_MFUART2_TXD — CH17 — GPP_F9/CNV_MFUART2_TXD
WWAN_BB_RST# — CF17 — GPP_F23/A4WP_PRESENT
1.8V only

GPP_H18/CPU_C10_GATE# — CN27 — GPPC_H18_VCCIO_LPM
GPP_H19/TIMESYNC0 — CM27
GPP_H21 — CF25 — GPP_H21
GPP_H22 — CN26
GPP_H23 — CM26 — GPP_H23
GPP_F10 — CK17
GPD7 — BV35 — GPD_7
GPP_F3 — CN20 — PROJECT_ID3
GPP_D4/IMGCLKOUT0/BK4/SBK4 — CG25 — WIFI_RF_EN
GPP_H20/IMGCLKOUT1 — CH25
GPP_F: VCCPGPPF = 1.8V Only

GPP_F12/EMMC_DATA0 — CR20
GPP_F13/EMMC_DATA1 — CM20
GPP_F14/EMMC_DATA2 — CN19
GPP_F15/EMMC_DATA3 — CM19
GPP_F16/EMMC_DATA4 — CN18
GPP_F17/EMMC_DATA5 — CR18
GPP_F18/EMMC_DATA6 — CP18
GPP_F19/EMMC_DATA7 — CM18
GPP_F20/EMMC_RCLK — CM16
GPP_F21/EMMC_CLK — CP16
GPP_F11/EMMC_CMD — CR16
GPP_F22/EMMC_RESET# — CN16
EMMC_RCOMP — CK15 — EMMC_RCOMP 1 R2108 2 200R2F-1-GP

ZZ.00CPU.271

WWAN_BB_RST

Power Management States for Modern connected standby platform

System States	USB device State	PCIe Device States	PCIe Link states	PERST#	PEWAKE#	CLKREQ#	BB_RESET#	Notes
S0	D0	D0	L0, L1.2	H	H	L0 : L L1.2 : H	H	
	D2	D3cold	L2	L	H	H	H	
S0ix	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem
S4	D2	D3cold	L2	L	H	H	H	
	D3cold	D3cold	L3	-	-	-	L	
S5	D3cold	D3cold	L3	-	-	-	L	Power is removed from modem

3D3V_S5_PCH
R2119 10KR2J-3-GP
WWAN_DB_DET#

1D8V_VCCPRIM
EMMC
R2111 Do Not Stuff
PROJECT_ID1
R2112 10KR2J-3-GP
nonEMMC

1D8V_VCCPRIM
VRAM_x32
R2113 10KR2J-3-GP
PROJECT_ID0
VRAM_x16
R2114 Do Not Stuff

1D8V_VCCPRIM
R2115 10KR2J-3-GP
PROJECT_ID3
R2116 DY Do Not Stuff

1D8V_VCCPRIM
R2117 10KR2J-3-GP
PROJECT_ID2
R2118 DY Do Not Stuff

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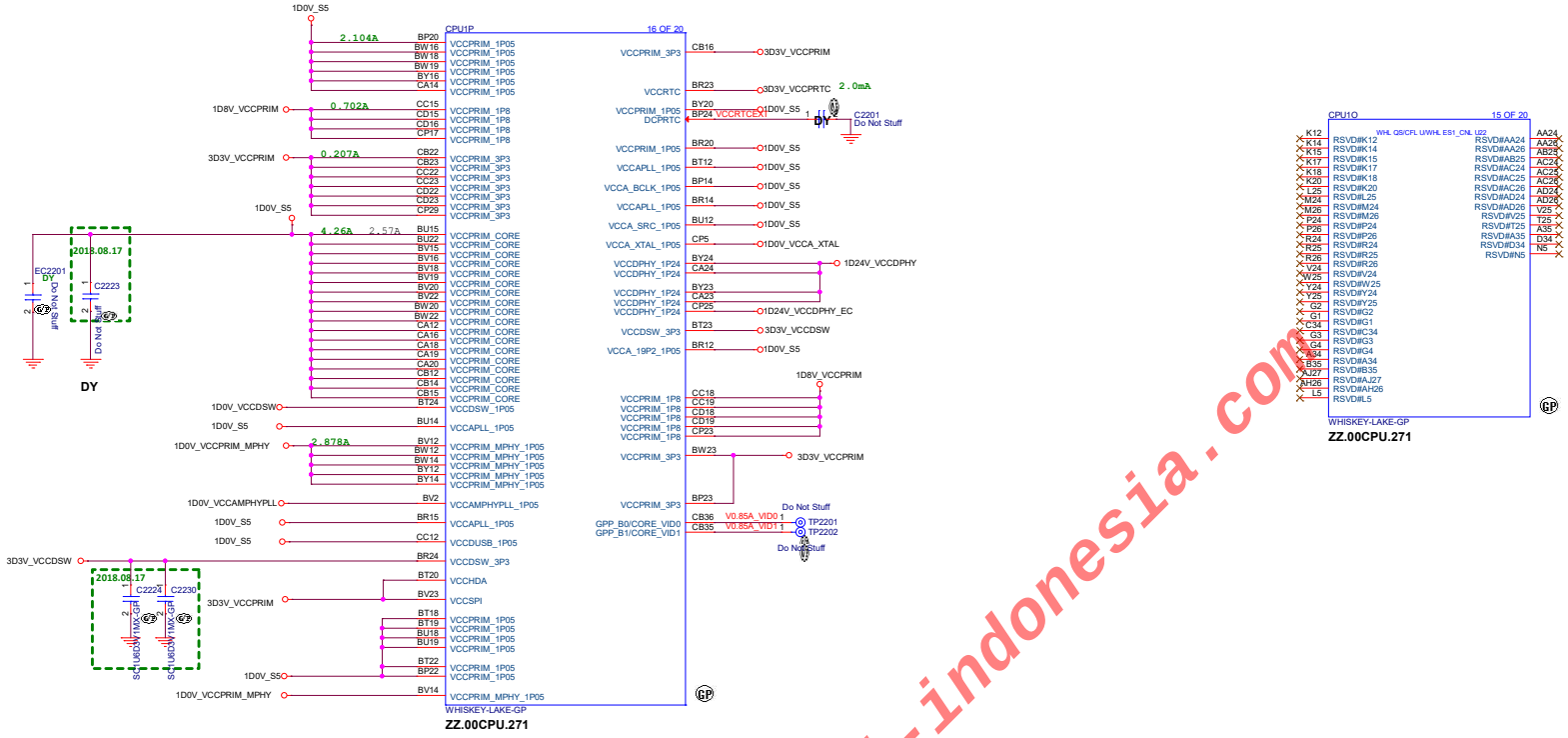
Title: CPU_(POWER1)
Size: A3 | Document Number: RogueOne 13" | Rev: A00
Date: Thursday, December 27, 2018 | Sheet 21 of 106

Main Func = CPU



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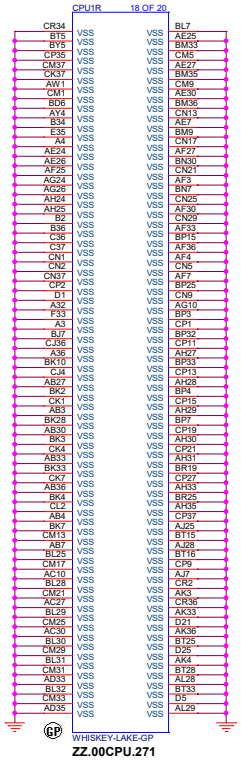
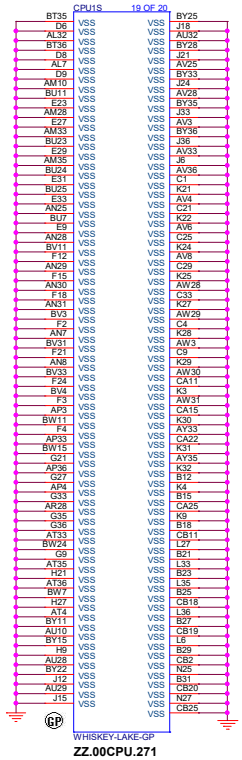
Title: CPU_(RSVD)

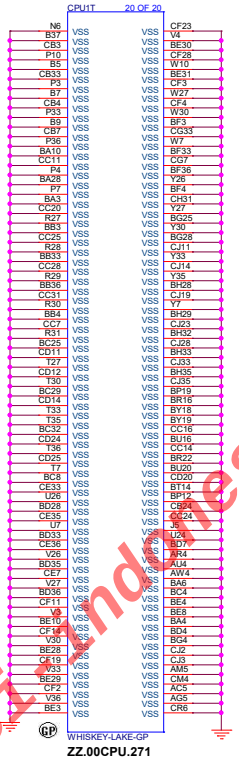
Size	Document Number	Rev
A2	RogueOne 13"	A00

Date: Thursday, December 27, 2018 Sheet 22 of 106

Main Func = CPU







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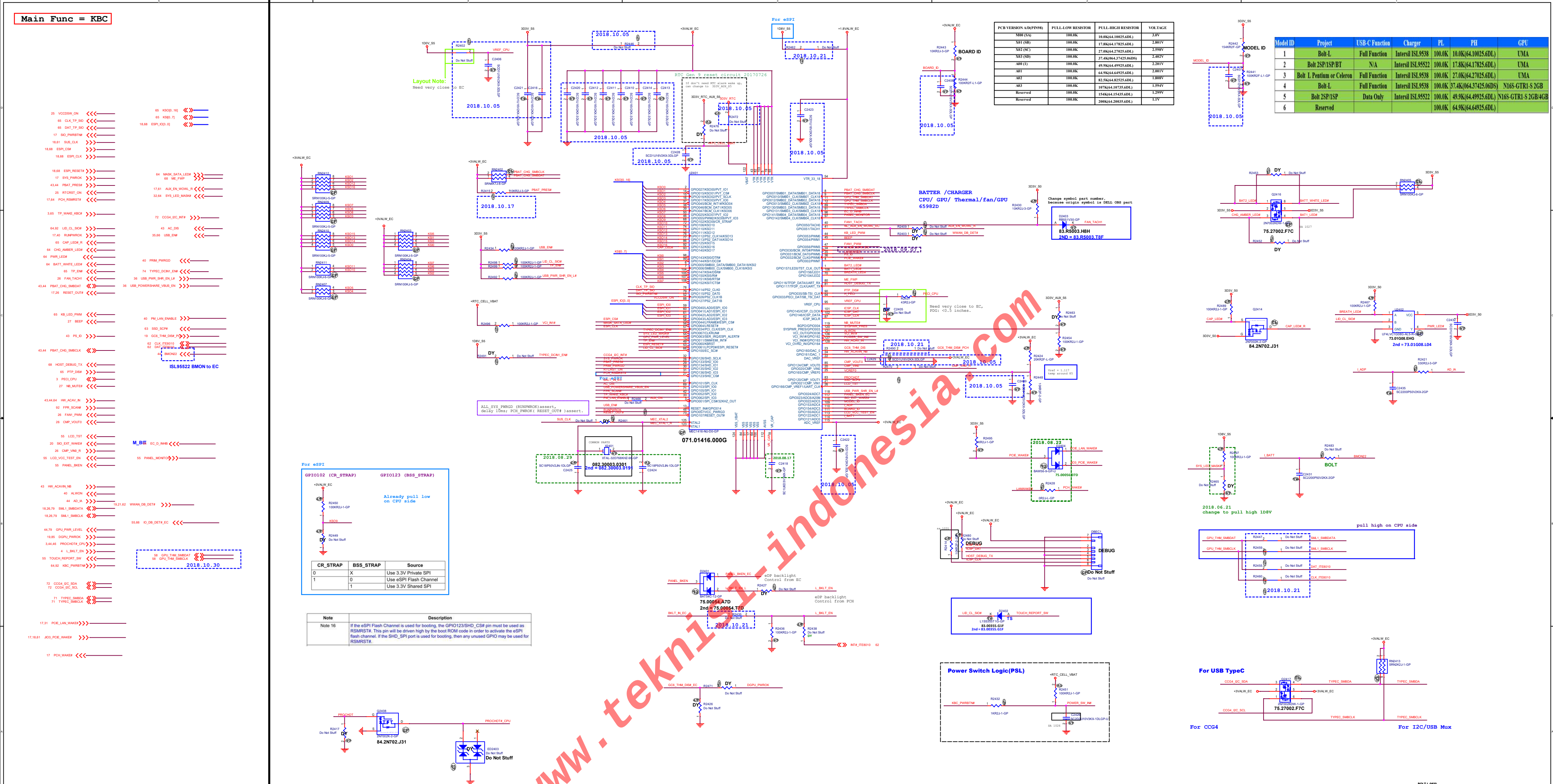
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_(VSS)

Size	Document Number	Rev
A2	RogueOne 13"	A00

Date: Thursday, December 27, 2018 Sheet 23 of 106

Main Func = KBC



PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
M00 (SA)	100.0K	10.0K(64.10025.6DL)	3.0V
X01 (SB)	100.0K	17.8K(64.17825.6DL)	2.801V
X02 (SC)	100.0K	27.0K(64.27025.6DL)	2.598V
X03 (SD)	100.0K	37.4K(064.37425.06DS)	2.402V
A00 (1)	100.0K	49.9K(64.49925.6DL)	2.201V
A01	100.0K	64.9K(64.64925.6DL)	2.001V
A02	100.0K	82.5K(64.82525.6DL)	1.808V
A03	100.0K	107K(64.10735.6DL)	1.594V
Reserved	100.0K	154K(64.15435.6DL)	1.299V
Reserved	100.0K	200K(64.20035.6DL)	1.1V

Model ID	Project	USB-C Function	Charger	PL	PH	GPU
1	Bolt-L	Full Function	Intersil ISL9538	100.0K	10.0K(64.10025.6DL)	UMA
2	Bolt 2SP/1SP/BT	N/A	Intersil ISL95522	100.0K	17.8K(64.17825.6DL)	UMA
3	Bolt L Pentium or Celeron	Full Function	Intersil ISL9538	100.0K	27.0K(64.27025.6DL)	UMA
4	Bolt-L	Full Function	Intersil ISL9538	100.0K	37.4K(064.37425.06DS)	N16S-GTR1-S 2GB
5	Bolt 2SP/1SP	Data Only	Intersil ISL95522	100.0K	49.9K(64.49925.6DL)	N16S-GTR1-S 2GB/4GB
6	Reserved			100.0K	64.9K(64.64925.6DL)	

For eSPI

GPIO102 (CR_STRAP) GPIO123 (BSS_STRAP)

Already pull low on CPU side

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

Note	Description
Note 16	If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE285PA0DX

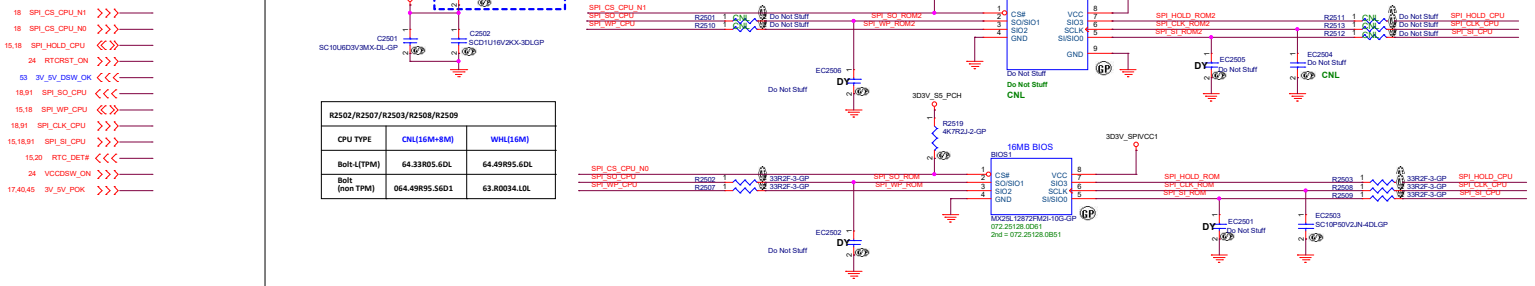
Size: Custom | Document Number: BOLT WHL | Rev: A00

Date: Thursday, December 27, 2018 | Sheet 24 of 106

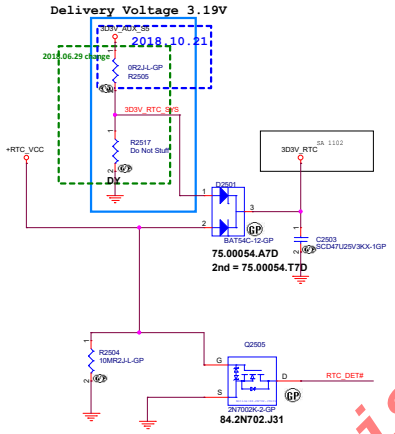
Main Func = SPI Flash

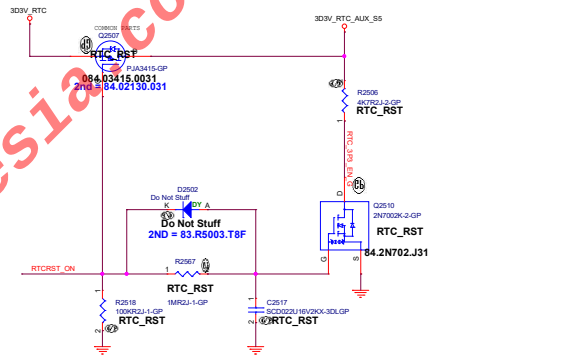
R2501/R2510/R2511/R2513/R2512		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt-L(TPM)	64.33R05.6DL	DY
Bolt (non TPM)	64.49R95.6DL	DY

R2502/R2507/R2503/R2508/R2509		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt-L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	064.49R95.56D1	63.R0034.L0L



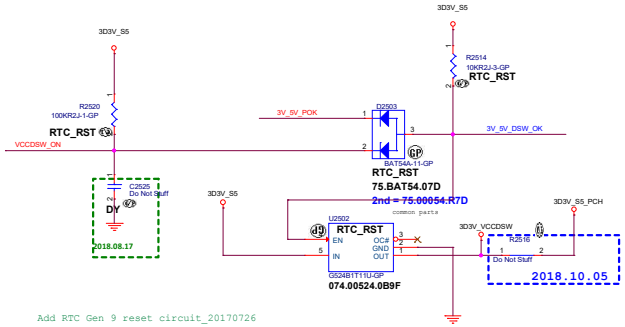
Main Func = RTC





29.2.1 VCCRTC External Circuit

On KBL, the VCCRTC max voltage is being reduced to minimize leakage on the ESD diodes and prevent RTC oscillator problems. Whether VCCRTC is sourced from Vbatt in G3 or VCCDSW_3p3 in Non-G3 state, platform designers must ensure the effective voltage at VCCRTC does not exceed 3.2V. The following sections will detail various options platform designers can use to achieve this new specification.



Add RTC Gen 9 reset circuit_20170726

BOLT L 0823

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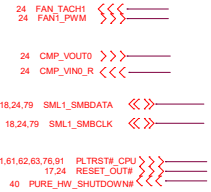
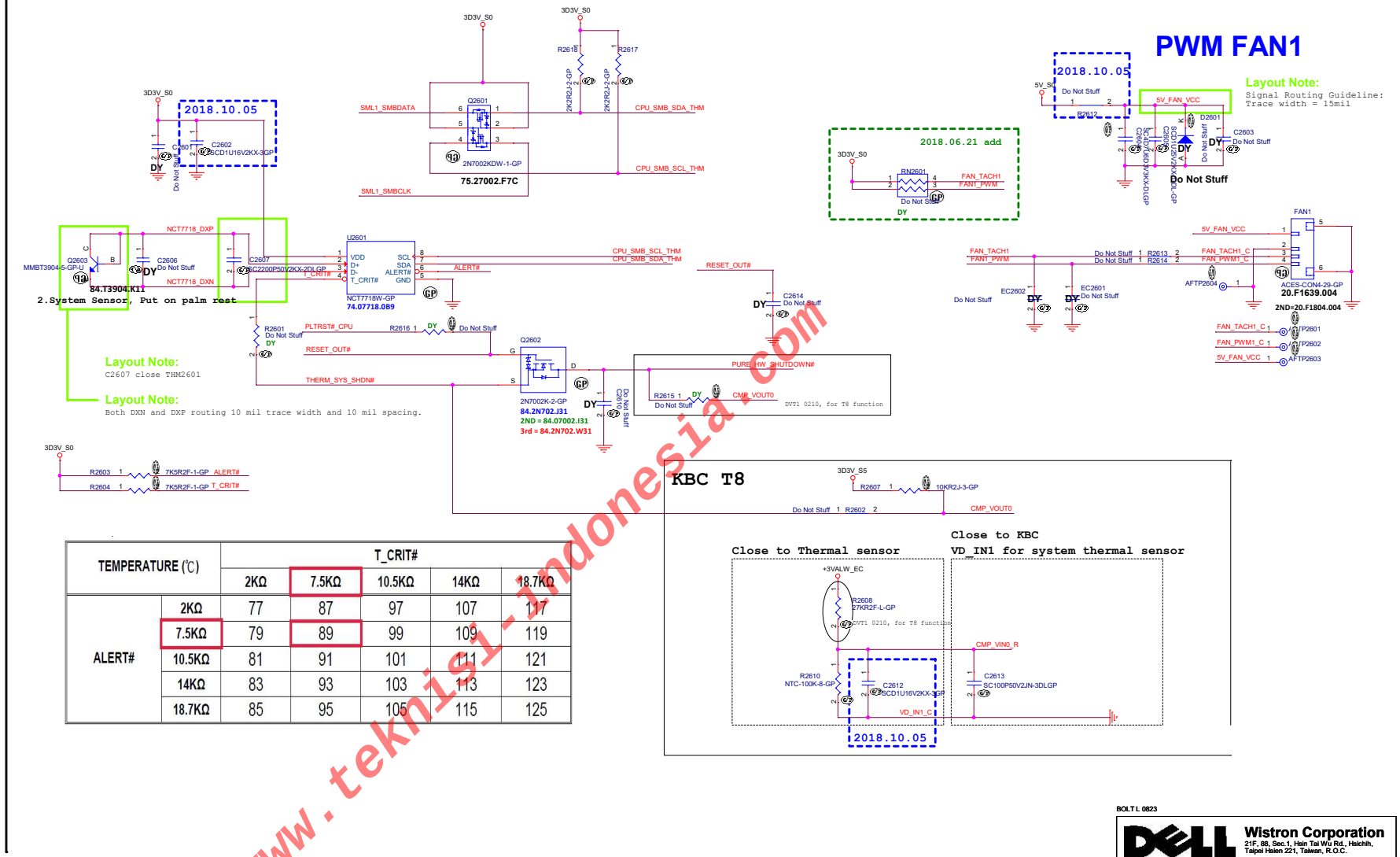
Taipei Hsien 221, Taiwan, R.O.C.

Title: Flash/RTC
Size: Custom | Document Number: BOLT WHL | Rev: A00
Date: Thursday, December 27, 2018 | Sheet 25 of 106

SSID = Thermal Sensor





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: THERMAL NCT7718W/Fan

Size: Custom | Document Number: BOLT WHL | Rev: A00

Date: Thursday, December 27, 2018 | Sheet 26 of 106

Main Func = Audio

< 2.5A (peak)
When play with 1KHz
sin wave on 2W/4ohm speaker

Analog
Digital

<50mA

Layout Note:
Place close to Pin 29

Layout Note:
Speaker trace
width >40mil @
2W4ohm speaker
power

DVDD must >= DVDD_IO

ALC3204
QFN40 (5x5)

ALC3204-CG-GP-U
071.03204.0003

moat

2018.10.05
2018.08.28
2018.10.21
2018.8.23
2018.05.03
FOR EMI
2018.09.03

place close to pin1
place close to pin8

Coin battery is used to solve the humming noise when UAJ port connecting to active speaker and system entering S3/S4/S5 or notebook battery mode or desktop G3 mode.

100K is used to speed up the discharge for LDO1. It could solve the pop sound during system boot up and reboot.

1.8V power rail should be supplied by linear regulator, not switching regulator.if switch regulator is unavilable, please make sure that switch frequency operates at out-band(over 20KHz)

BOLT L 0823	
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Audio Codec ALC3204
Size A2	Document Number BOLT WHL Rev A00
Date: Thursday, December 27, 2018	Sheet 27 of 105

(Blanking)

BOLT L 0823

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Title

(Reserved)

Size	Document Number	Rev
A4	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 28 of 105

Main Func = Audio

SPEAKER

27 AUD_SPK_R+
27 AUD_SPK_R-
27 AUD_SPK_L+
27 AUD_SPK_L-

Layout Note:
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

R2924 Do Not Stuff
R2925 Do Not Stuff
R2926 Do Not Stuff
R2927 Do Not Stuff

2018.10.05

SC1KP50V2KX-1DLGP EC2901
SC1KP50V2KX-1DLGP EC2902
SC1KP50V2KX-1DLGP EC2903
SC1KP50V2KX-1DLGP EC2904

AFTP2901
AFTP2902
AFTP2903
AFTP2904

SPK1
ACES-CON4-29-GP
20.F1639.004
2ND=20.F1804.004

CONN Pin	Net name
Pin1	SPK_L+_C
Pin2	SPK_L-_C
Pin3	SPK_R+_C
Pin4	SPK_R-_C
Pin5	GND
Pin6	SPK_DET#_CON

Audio Jack

Layout Note: Should be placed nearby codec IC (HDA27).

RN2901 SRN2K2J-1-GP
C2907 SC4D7U6D3V3KX-DLGP
C2908 SC4D7U6D3V3KX-DLGP
R2922 1KR2J-1-GP
R2921 1KR2J-1-GP
D2901 BAT54A-11-GP
75.BAT54.07D
R2912 4K7R2J-2-GP
R2913 4K7R2J-2-GP
R2908 10R2F-L1-GP
R2910 10R2F-L1-GP

EC2908 SC1KP50V2KX-2DLGP
EC2907 SC680P50V2KX-2DLGP
EC2905 SC1KP16V2KX-DLGP
EC2906 SC1KP16V2KX-DLGP

2018.08.28
2018.08.28

2018.10.05
R2906 Do Not Stuff
R2907 Do Not Stuff
R2909 Do Not Stuff
R2911 Do Not Stuff

Universal Jack
HPMIC1
AUDIO-JK677-GP

Delay circuit
(JACK_PLUG_DET: on I/O Board)
R2923 Do Not Stuff
2018.10.21
C2902 Do Not Stuff

R2914 Do Not Stuff
2018.10.21

CLOSS TO HPMIC1
ED2910 AZ5125-02S-R7G-GP 75.05125.07D
ED2911 AZ5125-02S-R7G-GP 75.05125.07D
ED2912 AZ5125-02S-R7G-GP 75.05125.07D

moat

SCHEMATIC
#3 G/M
#1 L
#5
#6
#2 R
#4 M/G

BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/Universal Jack
Size: Custom
Document Number: BOLT WHL
Rev: A00
Date: Thursday, December 27, 2018
Sheet 29 of 105

(Blanking)

BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

(Reserved)

Size	Document Number	Rev
A4	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 30 of 105

Main Func = LAN

LAN CHIP (10/100/1000M & 10/100M co-lay)

PCIE

16 LAN_PCIE_TX_P
16 LAN_PCIE_TX_N
16 LAN_PCIE_RX_P
16 LAN_PCIE_RX_N

PCIE_CLK

18 LAN_CLK_CPU_P
18 LAN_CLK_CPU_N
18 CLK_PCIE_LAN_REQ#

MDI

32 LAN_MDI0_P
32 LAN_MDI0_N
32 LAN_MDI1_P
32 LAN_MDI1_N
32 LAN_MDI2_P
32 LAN_MDI2_N
32 LAN_MDI3_P
32 LAN_MDI3_N

17,24 PCIE_LAN_WAKE#
17,26,61,62,63,76,91 PLTRST#_CPU

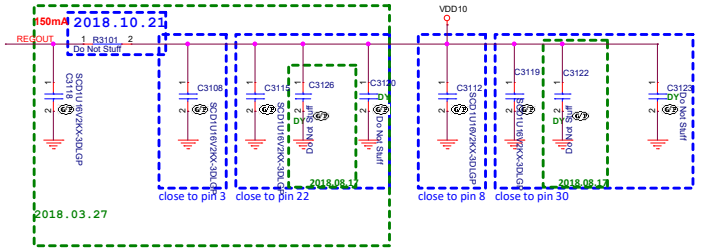
19 LOM_CABLE_DETECT#

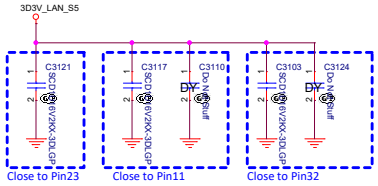
32 LAN_LED0

3D3V_LAN_S5 rise time must be controlled between 0.5 mS and 100 mS.

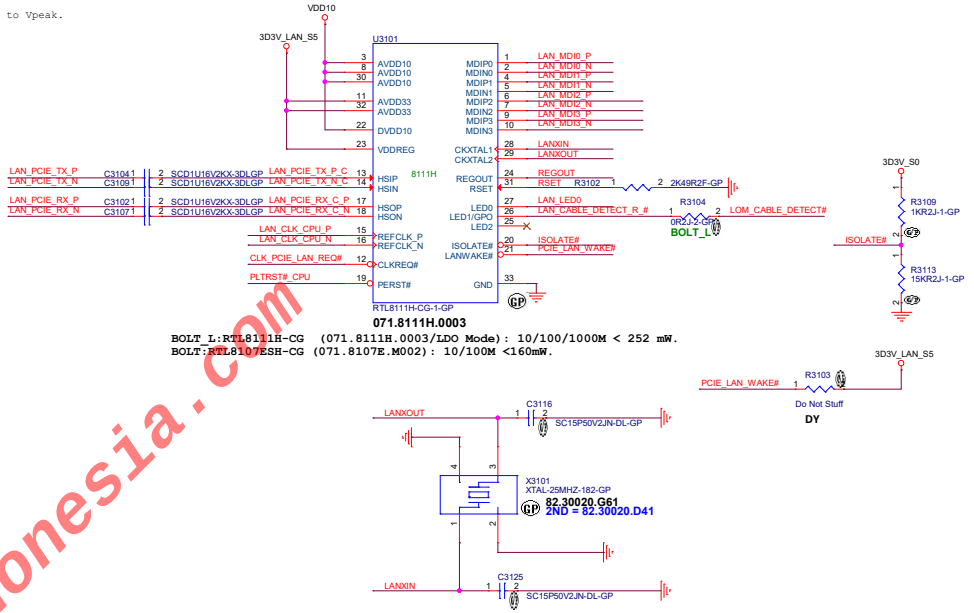
LAN power Noise 3.3V < 200mV Vpeak to Vpeak.

LAN power Noise 1.0V < 100mV Vpeak to Vpeak.





C3110/C3124 for surge



BOLT_L:RTL8111H-CG (071.8111H.0003/LDO Mode): 10/100/1000M < 252 mW.
BOLT:RTL8107ESH-CG (071.8107E.M002): 10/100M <160mW.

BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

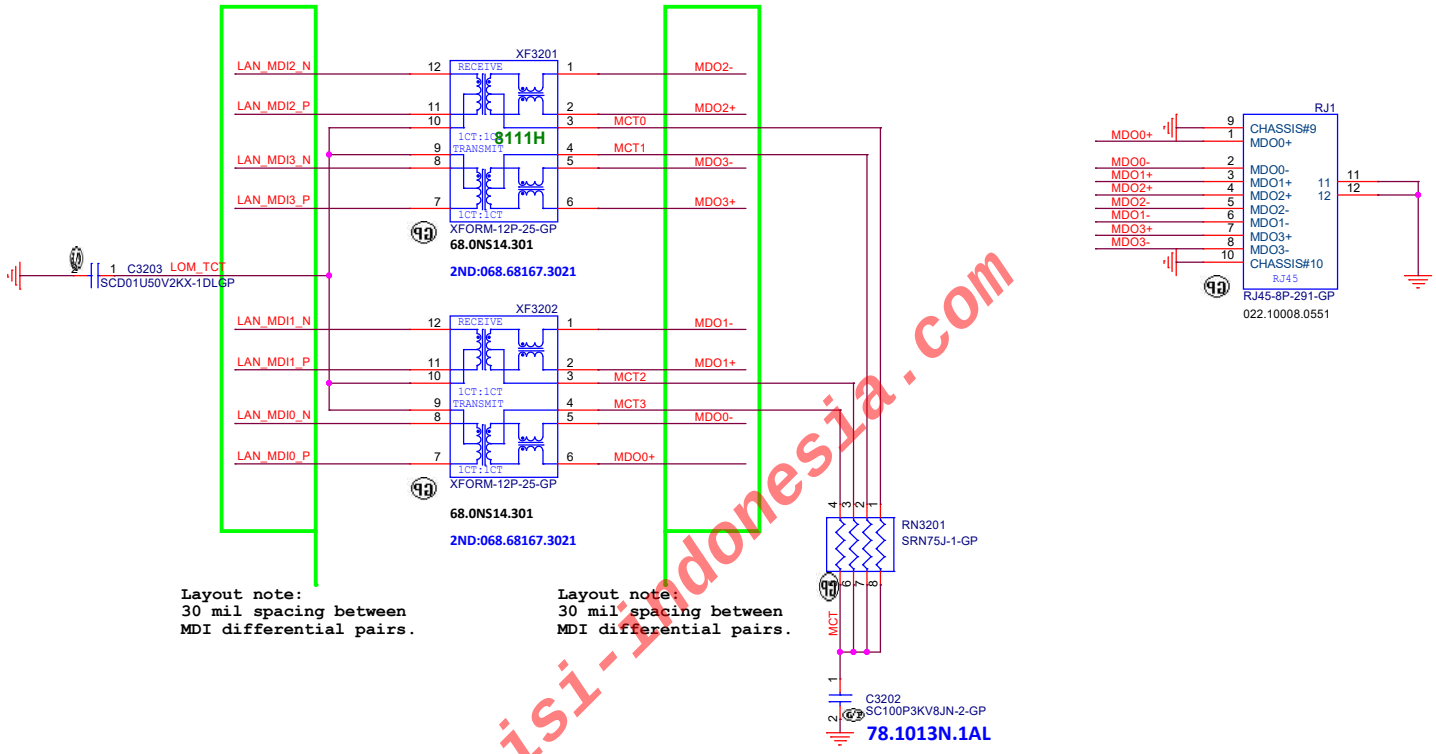
Title: LAN RTL8106

Size: Custom | Document Number: BOLT WHL | Rev: A00

Date: Thursday, December 27, 2018 | Sheet 31 of 105

Main Func = LAN

LAN TransFormer (10/100/1000M & 10/100M co-lay)



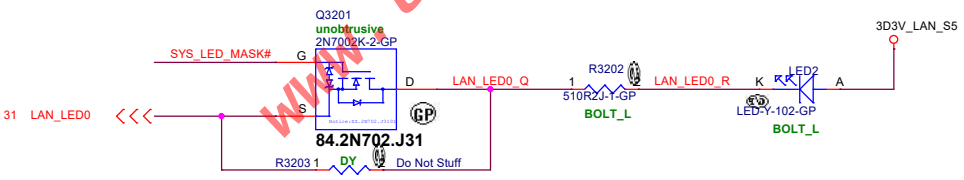
MDI

31 LAN_MDI0_P
31 LAN_MDI0_N
31 LAN_MDI1_P
31 LAN_MDI1_N
31 LAN_MDI2_P
31 LAN_MDI2_N
31 LAN_MDI3_P
31 LAN_MDI3_N

24,64 SYS_LED_MASK#

Green LED Status:
Blinking:Data transmit (10/100/1000)
Always Turn On: Network Connection exist
Turn Off: No network connection exist

LED

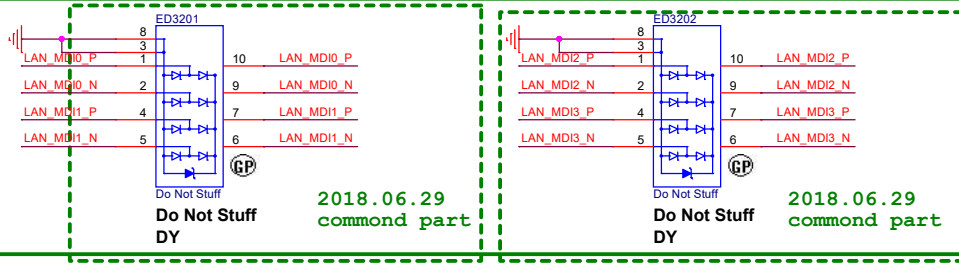


TEST PAD

Layout:
Place near RJ45

Do Not Stuff AFTP3204 MDO0+
Do Not Stuff AFTP3201 MDO0-
Do Not Stuff AFTP3202 MDO1+
Do Not Stuff AFTP3208 MDO1-
Do Not Stuff AFTP3205 MDO2+
Do Not Stuff AFTP3207 MDO2-
Do Not Stuff AFTP3209 MDO3+
Do Not Stuff AFTP3206 MDO3-

ESD



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Title: XFOM&RJ45
Size: A3
Document Number: BOLT WHL
Rev: A00
Date: Thursday, December 27, 2018
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BOLT L 0823

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Card Reader Re-driver

Size	Document Number	Rev
A2	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 33 of 105

(Blanking)

BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB2.0 CONN

Size | Document Number: BOLT WHL | Rev: A00

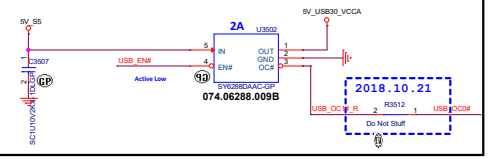
Date: Thursday, December 27, 2018 | Sheet 34 of 105

Main Func = USB 3.0

USB Power Switch Enable

24,66 USB_EN#
16,36 USB_OC0#

USB Power Switch



USB Power Sharing

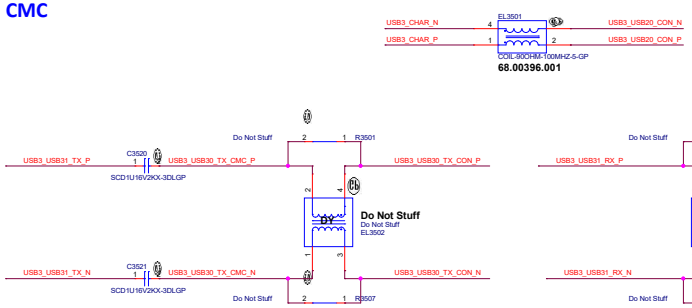
3.1 阻值範圍: ≥ 1Ω & 0Ω

型別	額定功率	最高額定電壓	最高過負荷電壓	T.C.R (ppm/°C) 溫度係數	阻值範圍 B(±0.1%) E-24 ~ E-96	D(±0.5%) E-24 ~ E-96	F(±1%) E-24 ~ E-96	G(±2%) ~ J(±5%) E-24	JUMPER (0Ω) 額定電流 J (±5%)	JUMPER (0Ω) 額定電流 F (±1%)	JUMPER (0Ω) 阻值 J (±5%)	JUMPER (0Ω) 阻值 F (±1%)
RT701 (0201)	1/20 W	25V	50V	-200 ~ +400	------	10Ω≦R<100Ω	10Ω≦R<100Ω	10Ω≦R<100Ω	0.5A	0.5A	50mΩ MAX.	35mΩ MAX.
				±200	47Ω≦R≦1MΩ	100Ω≦R≦10MΩ	100Ω≦R≦10MΩ	100Ω≦R≦10MΩ				
RT702 (0402)	1/16 W	50V	100V	±100	100Ω≦R≦1MΩ	100Ω≦R≦1MΩ	100Ω≦R≦22MΩ	100Ω≦R≦22MΩ	1A	1.5A	50mΩ MAX.	20mΩ MAX.
				±200	------	------	10Ω≦R<100Ω	10Ω≦R<100Ω				
RT703 (0603)	1/10 W	75V	150V	±100	100Ω≦R≦1MΩ	100Ω≦R≦1MΩ	100Ω≦R≦22MΩ	100Ω≦R≦22MΩ	1A	2A	50mΩ MAX.	20mΩ MAX.
				±200	------	------	10Ω≦R<100Ω	10Ω≦R<100Ω				
RT705 (0805)	1/8 W	150V	300V	±100	100Ω≦R≦1MΩ	100Ω≦R≦10MΩ	100Ω≦R≦27MΩ	100Ω≦R≦27MΩ	2A	2.5A	50mΩ MAX.	20mΩ MAX.
				±200	------	10Ω≦R<100Ω	10Ω≦R<100Ω	10Ω≦R<100Ω				

USB2.0 from USB Charger

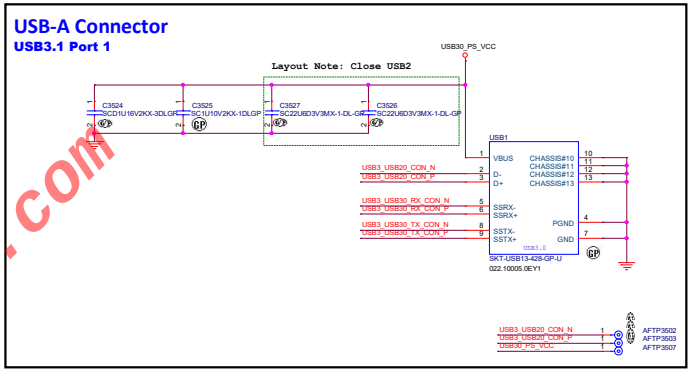
36 USB3_CHAR_N
36 USB3_CHAR_P

CMC



USB-A Connector

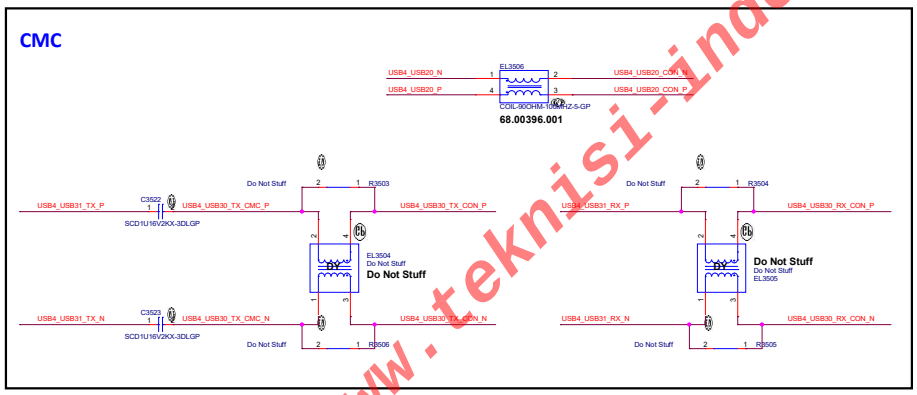
USB3.1 Port 1



USB2.0

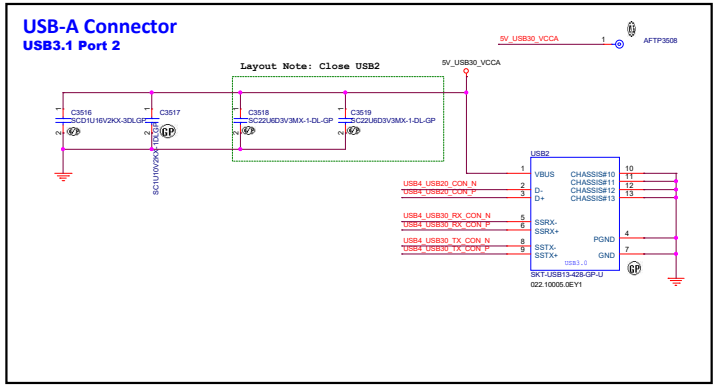
16 USB4_USB20_N
16 USB4_USB20_P

CMC



USB-A Connector

USB3.1 Port 2

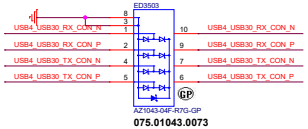


USB3.1

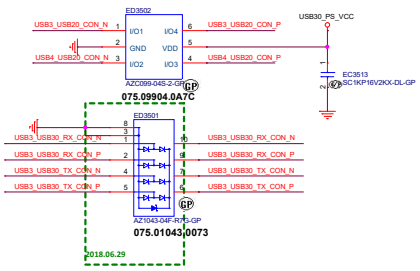
16 USB3_USB31_TX_P
16 USB3_USB31_TX_N
16 USB3_USB31_RX_P
16 USB3_USB31_RX_N

16 USB4_USB31_TX_P
16 USB4_USB31_TX_N
16 USB4_USB31_RX_P
16 USB4_USB31_RX_N

ESD FOR PORT1



ESD FOR PORT2



BOLT L 0823

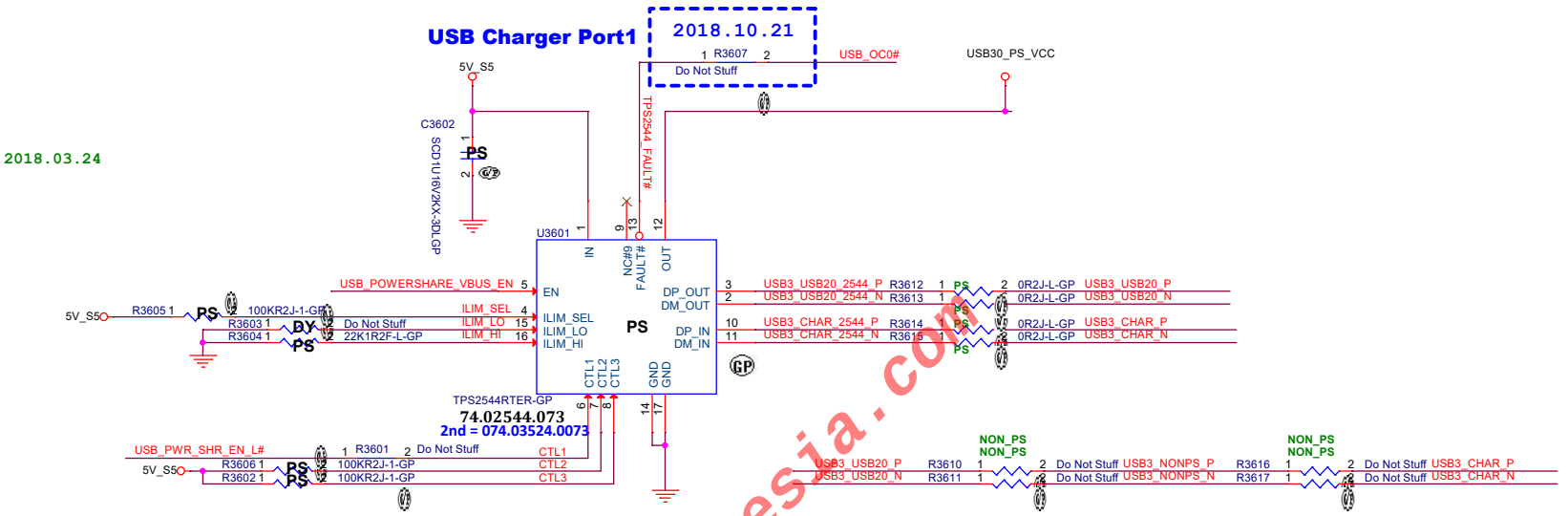
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.0 CONN

Size: Custom | Document Number: BOLT WHL | Rev: A00

Date: Thursday, December 27, 2018 | Sheet 35 of 105

Main Func = USB Charger



Device Control Pins				
	CTL1 (EC control)	CTL2	CTL3	ILIM_SEL
CDP	1	1	1	1
DCP Auto	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_typ}\,(mA) = \frac{50{,}500}{(R_{ILIM\_XX}\,(k\Omega) + 0.1)}$$

R_{ILIM_XX} corresponds to either R_{ILIM_HI} or R_{ILIM_LO} as appropriate.

35 USB3_CHAR_P
35 USB3_CHAR_N
16 USB3_USB20_P
16 USB3_USB20_N
24 USB_POWERSHARE_VBUS_EN
24 USB_PWR_SHR_EN_L#
16,35 USB_OC0#

BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB Charger
Size: Custom | Document Number: BOLT WHL | Rev: A00
Date: Thursday, December 27, 2018 | Sheet 36 of 105

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BOLT L 0823

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

USB3.0 PORT

Size	Document Number	Rev
A4	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 37 of 105

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BOLT L 0823

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB3.1 GEN-2 Redriver

Size	Document Number	Rev
A2	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 38 of 105

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BOLT L 0823

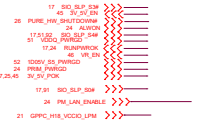
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: (RSVD)

Size	Document Number	Rev
A2	BOLT WHL	A00

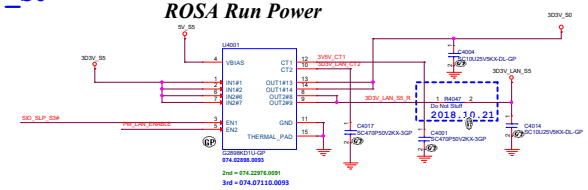
Date: Thursday, December 27, 2018 Sheet 39 of 105

Main FUNC = Power Plane & Sequence

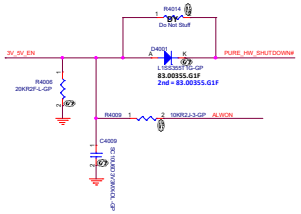


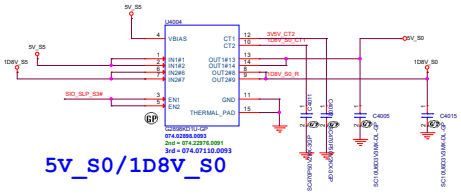
3D3V_S0/5V_S0

ROSA Run Power



3D3V_S0/LAN POWER





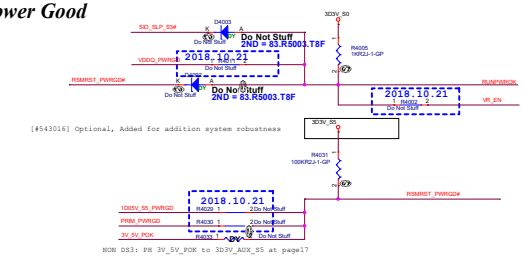
5V_S0/1D8V_S0

Table 4. Rise Time Values

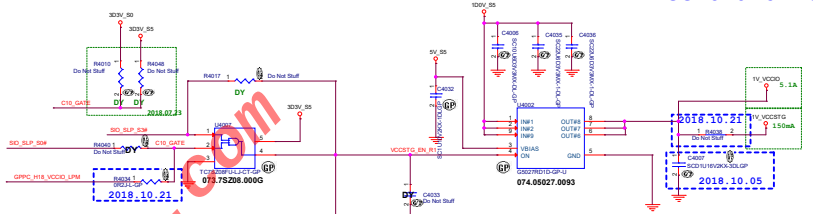
CT (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω[1]						
	5 V	3.3 V	1.8 V	1.5 V	1.2 V	1.05 V	0.6 V
0	149	112	77	70	60	56	42
220	548	388	236	206	173	154	103
470	968	673	401	342	289	256	169
1000	1768	1220	711	608	505	445	286
2200	3916	2678	1554	1332	1097	949	627
4700	8040	5477	3179	2691	2240	1964	1249
10000	16520	11150	6410	5401	4430	3933	2526

(1) TYPICAL VALUES at 25°C, V_{BIAS} = 5 V, 25 V X7R 10% CERAMIC CAP

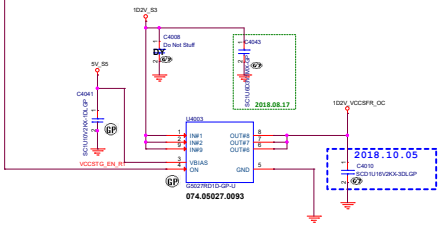
Power Good



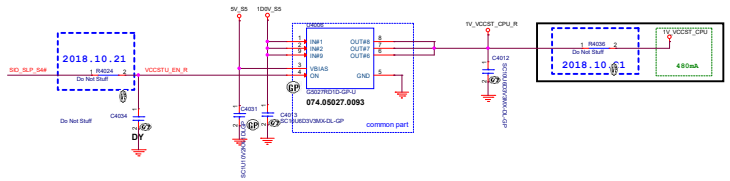
VCCIO and VCCSTG



VCCSPLL_OC



VCCST/VCCPLL



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Title: **Power Plane Enable**

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A3	BOLT WHL	A00

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Title: *Sequence (Modern_Standby)*

Size	Document Number	Rev
A4	BOLT WHL	A00

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Title: *Connected_Standby(2/2)*

Size	Document Number	Rev
A4	BOLT WHL	A00

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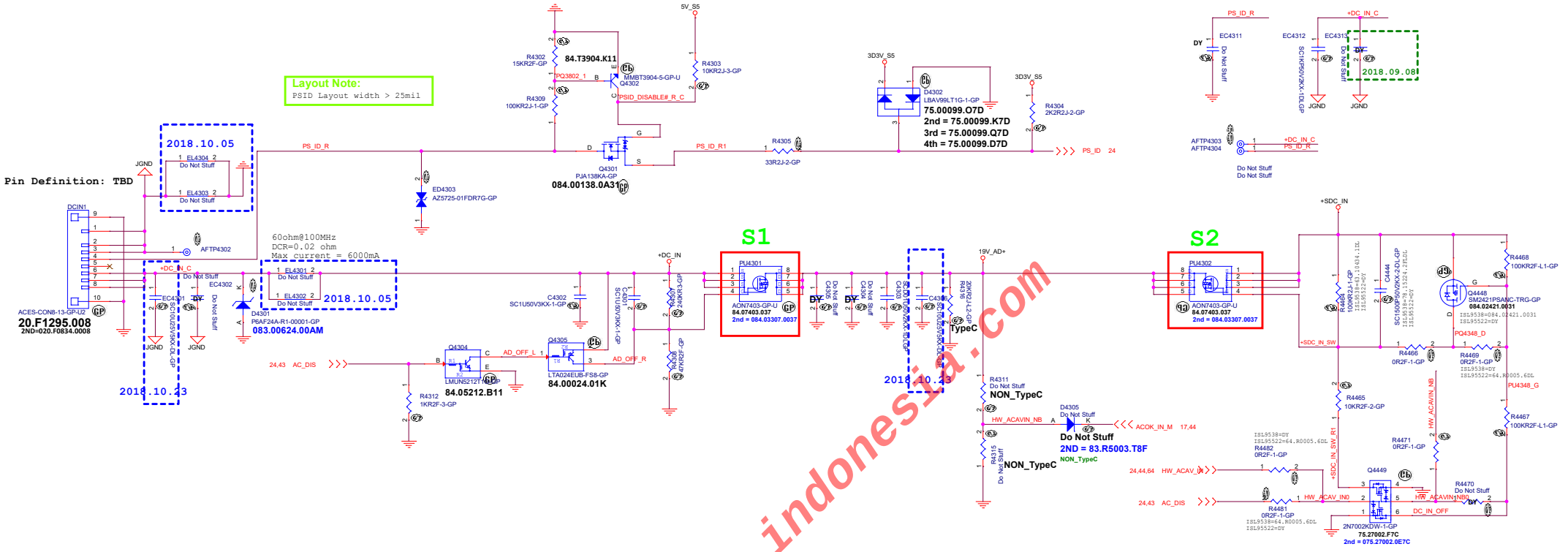
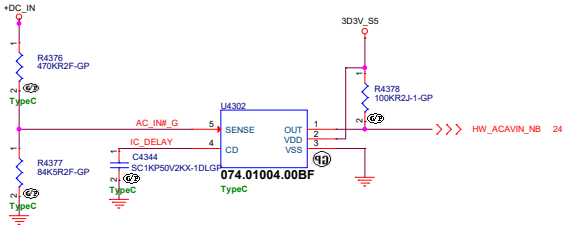
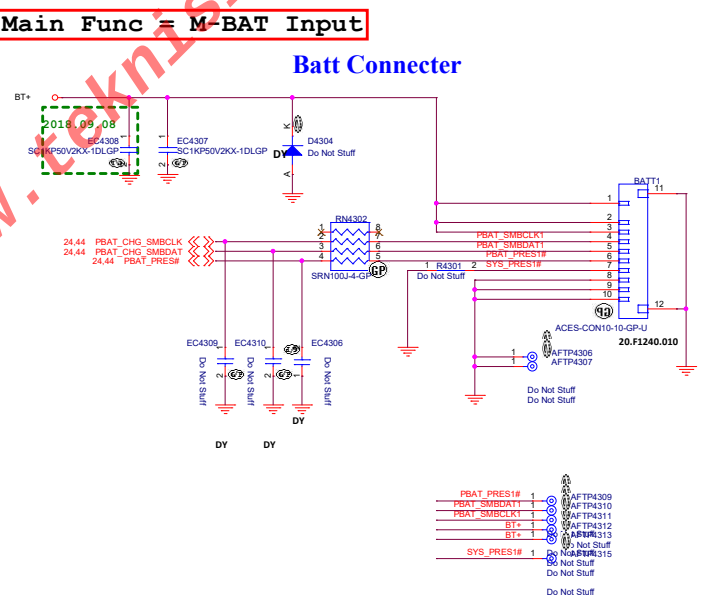
Main Func = ADT Input

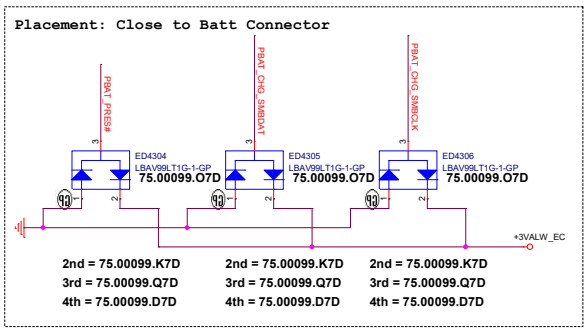


Main Func = Barrel Adapter Piug-in Detect



Main Func = M-BAT Input





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Title		
DCIN		
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Main Func = Charger

ISL95522 Hybrid Charger

Default **ISL9538 Buck-Boost Charger**

OFF PAGE

I2C form EC

To EC

ISL95522 BMON to EC

ISL9538 AMON/BMON to EC
ISL95522 AMON to EC

From MXP ACE

TypeC Prochot
Follow custormer circuits.

CHECK EE
follow custormer circuits.

PU +VCCSTG = 1.0 V on CPU side

PU 3V3_AON_S0 on GPU side

BOM Change List

ISL9538

TABLE 22. PROG PIN PROGRAMMING OPTIONS

PROG-GND RESISTANCE (kΩ)			CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT ADLimit1 Reg(A)
MIN	TYP ±1%	MAX				
	0		1	733kHz	No	0.476
	8.45			733kHz	No	1.5
	14.7			1MHz	No	1.5
	21.0			1MHz	No	0.476
	28.0			733kHz	Yes	0.476
	35.7			733kHz	Yes	1.5
	43.2		2	733kHz	Yes	1.5
	52.3			733kHz	No	0.476
	61.9			1MHz	No	0.476
	71.5			1MHz	No	1.5
	82.5			733kHz	No	1.5
	93.1			733kHz	No	0.476
	105		3	733kHz	No	0.476
	118			733kHz	No	1.5
	133			1MHz	No	1.5
	147			1MHz	No	0.476
	162			733kHz	Yes	0.476
	178			733kHz	Yes	1.5
	196		4	733kHz	Yes	1.5
	215			733kHz	No	0.476
	237			1MHz	No	0.476
	261			1MHz	No	1.5
	287			733kHz	No	1.5
	316			733kHz	No	0.476
	348		1	733kHz	No	0.476

ISL95522

Table 17. Prog Pin Programming Options

Prog-GND Resistance (kΩ)			
Typ (1% Standard Resistor)	Charger Type	Current Sense Resistor Value	Default # of Battery Cells in Series
0	NVDC	R_{S1} / R_{S2} = 2:1	3
22.6		R_{S1} = 10mΩ R_{S2} = 5mΩ or R_{S1} = 20mΩ R_{S2} = 10mΩ	4
38.3			2
69.8		R_{S1} / R_{S2} = 1:1 R_{S1} = 10mΩ R_{S2} = 10mΩ or R_{S1} = 20mΩ R_{S2} = 20mΩ	3
86.6			4
102			2
150	HPB		4
165			2
182			3
215		R_{S1} / R_{S2} = 2:1 R_{S1} = 10mΩ R_{S2} = 5mΩ or R_{S1} = 20mΩ R_{S2} = 10mΩ	4
237			2
255			3

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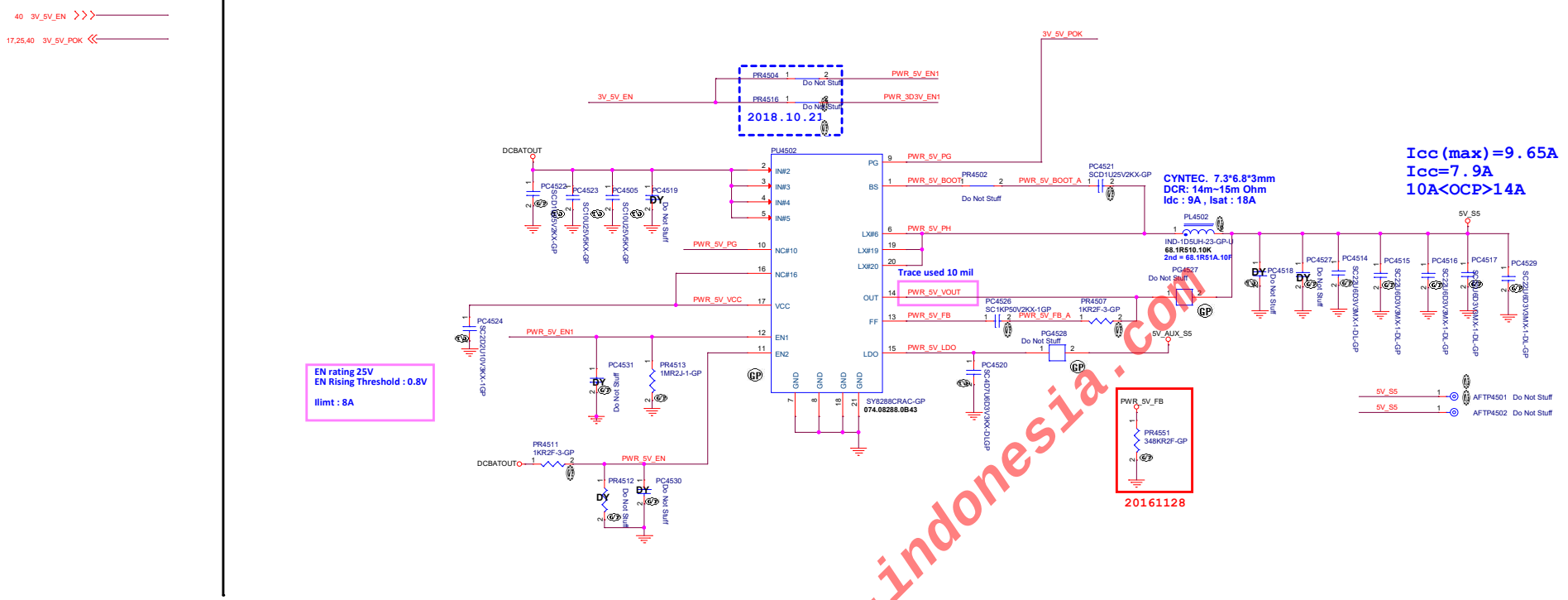
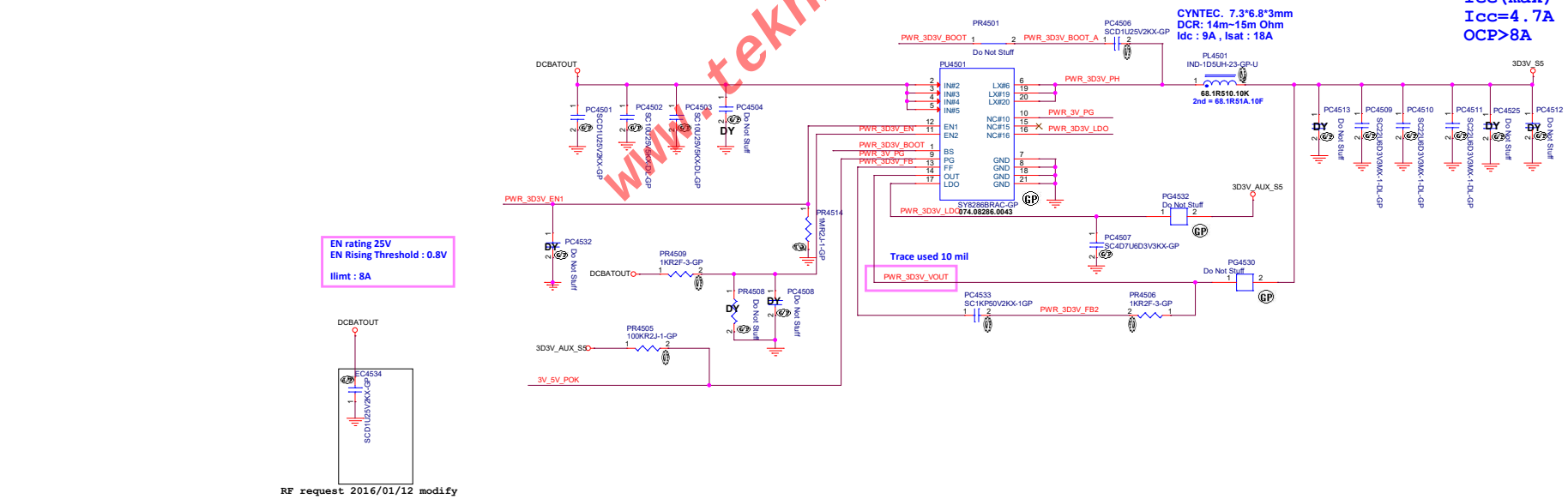
Charger

BOLT WHL

Main FUNC = PWR.Plane.Regulator_5V



Main FUNC = PWR.Plane.Regulator_3D3V



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Title: (Reserved)

Size	Document Number	Rev
A2	BOLT WHL	A00

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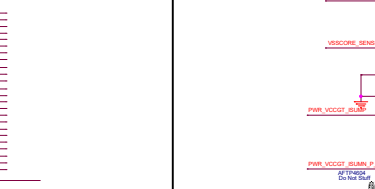
Main Func = CPU_CORE



	U22	U42	
PC4614	330P(78.33124.2FLDL)	470p(78.47124.2FLDL)	
PC4618	1KP(78.10224.2FLDL)	470p(78.47124.2FLDL)	2017/04/25
PC4625	DY	0.022u(78.22321.2FLDL)	
PC4626	DY	0.022u(78.22321.2FLDL)	
PR4669	DY	DY	2017/02/21
PR4670	1K(64.10015.6DL)	DY	
PR4642	357(64.35705.6DL)	523 (64.52305.6DL)	2018/04/27
PC4630	47nF(078.47322.02FD)	47nF(078.47322.02FD)	
PC4628	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)	
PC4654	22nF(78.22321.2FLDL)	22nF(78.22321.2FLDL)	2018/08/06
PC4653	DY	47nF(078.47322.02FD)	
PR4633	1.54K(64.15415.6DL)	2.55K(64.25515.6DL)	
PR4608	90.9K(64.90925.6DL)	100K (64.10035.6DL)	2018/04/27

WHL_U42_15W
VCORE Icc(max)=70A TDC=48 A
VCCGT Icc(max)=31A TDC=18 A
VCCSA Icc(max)=6A TDC=4A

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NCP81208MN_CPU_VCORE(1/3)

Size: A1 | Document Number: BOLT WHL | Rev: A00

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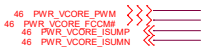
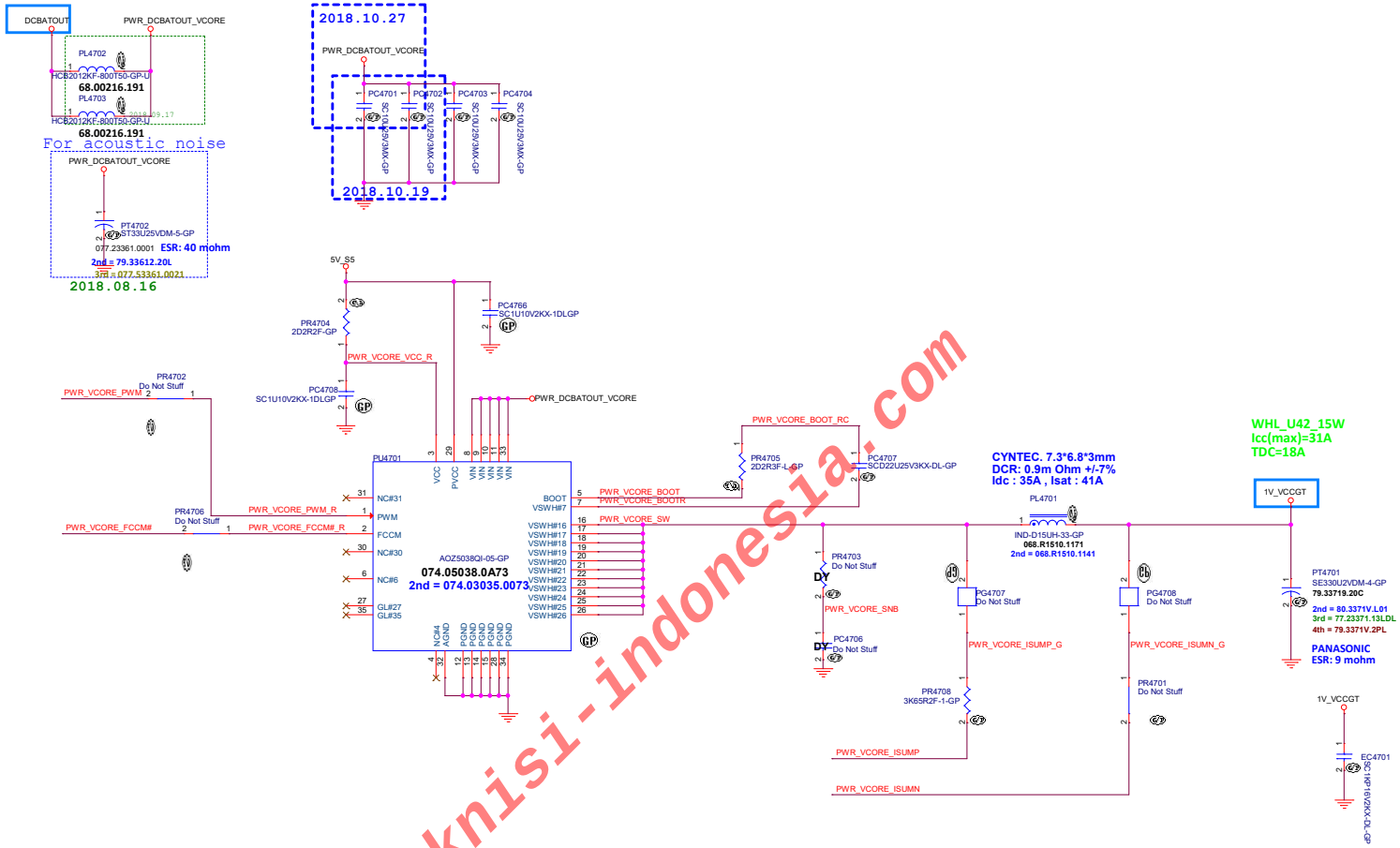
Main FUNC = CPU_CORE





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Title: NCP81382MN_CPU_VCORE(2/3)

Size: A2 | Document Number: BOLT WHL | Rev: A00

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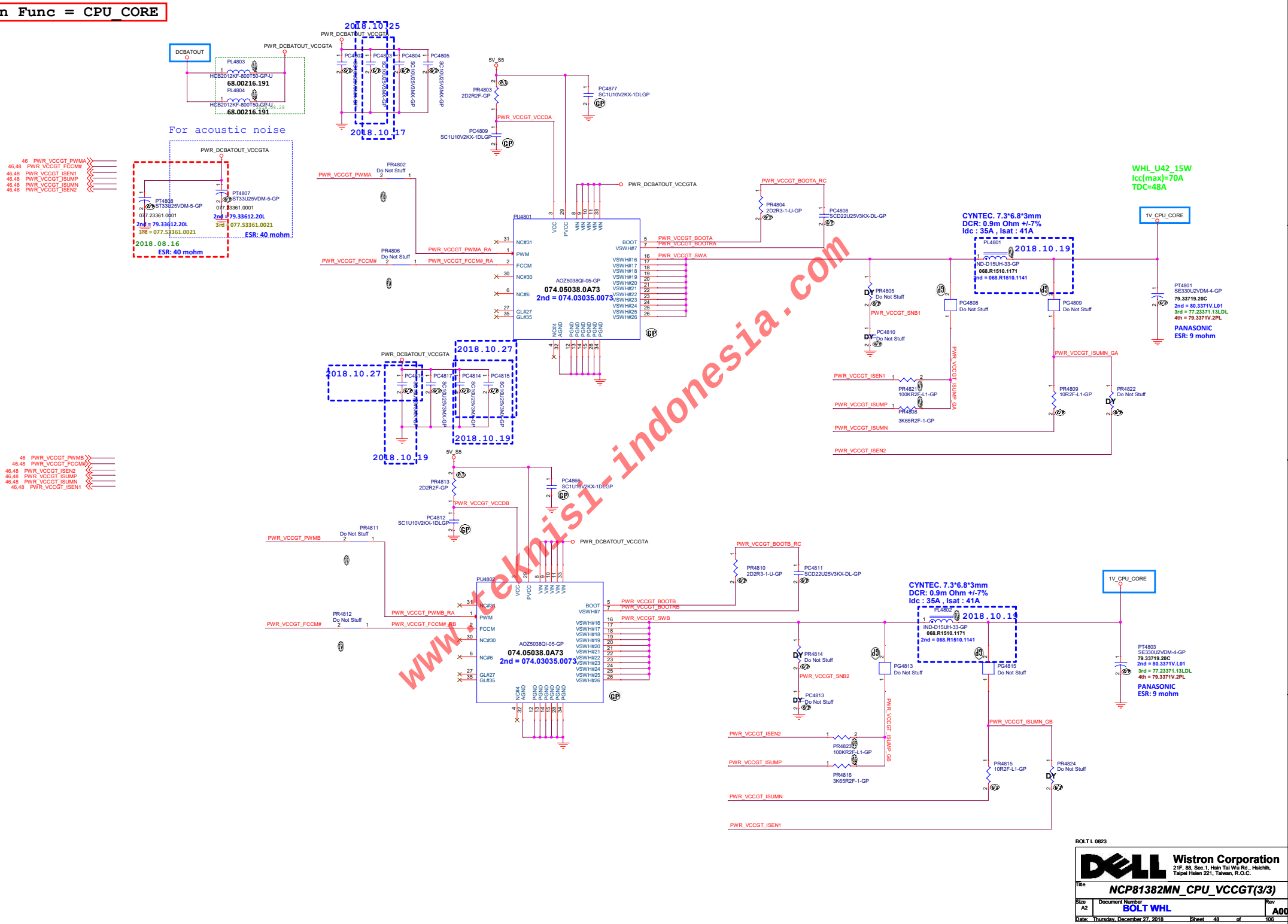
Main Func = CPU_CORE



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Title: NCP81382MN_CPU_VCCGT(3/3)

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A2	BOLT WHL	A00

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Title: NCP81210MN_CPU_VCCGTUS

Size	Document Number	Rev
A4	BOLT WHL	A00

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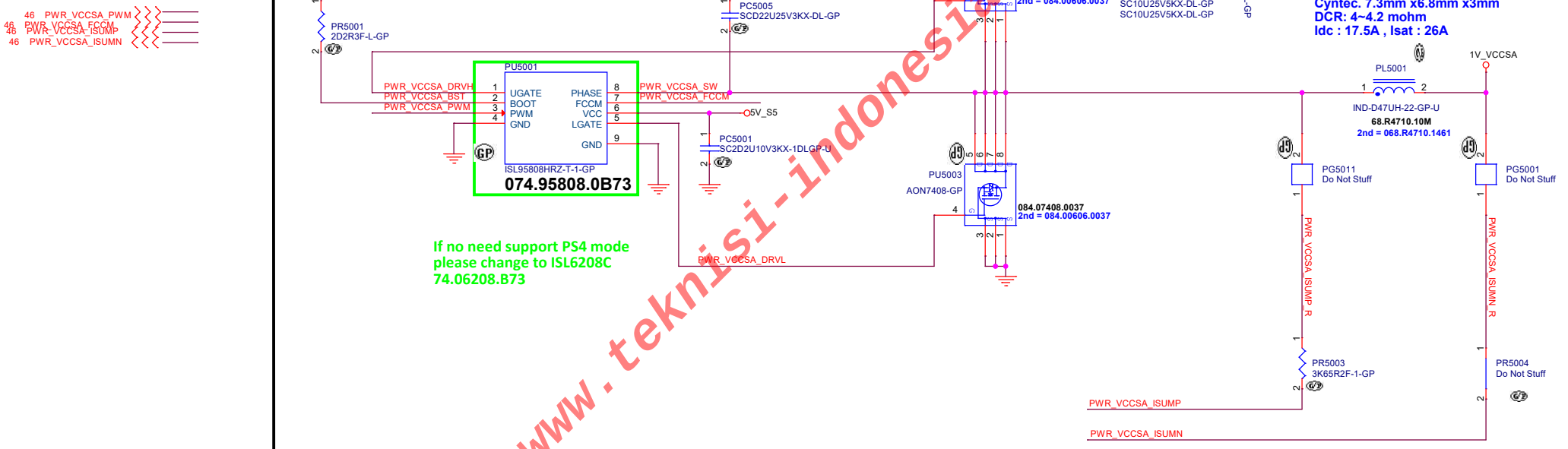
Main FUNC = CPU_CORE



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Title: VCCSA

Size: A3 | Document Number: BOLT WHL | Rev: A00

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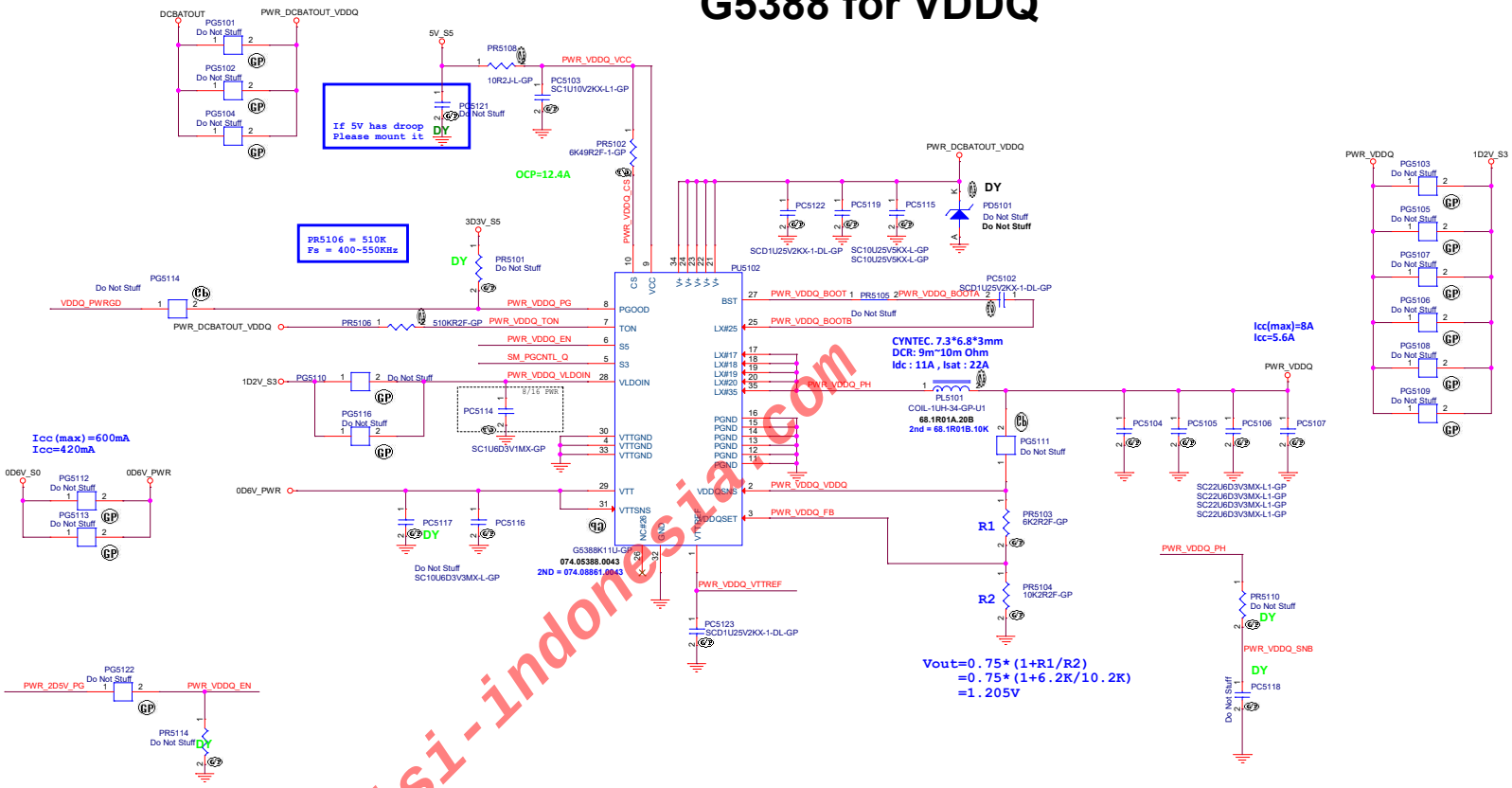
Main Func = PWR.Plane.Regulator_1D2V/0D6V

G5388 for VDDQ



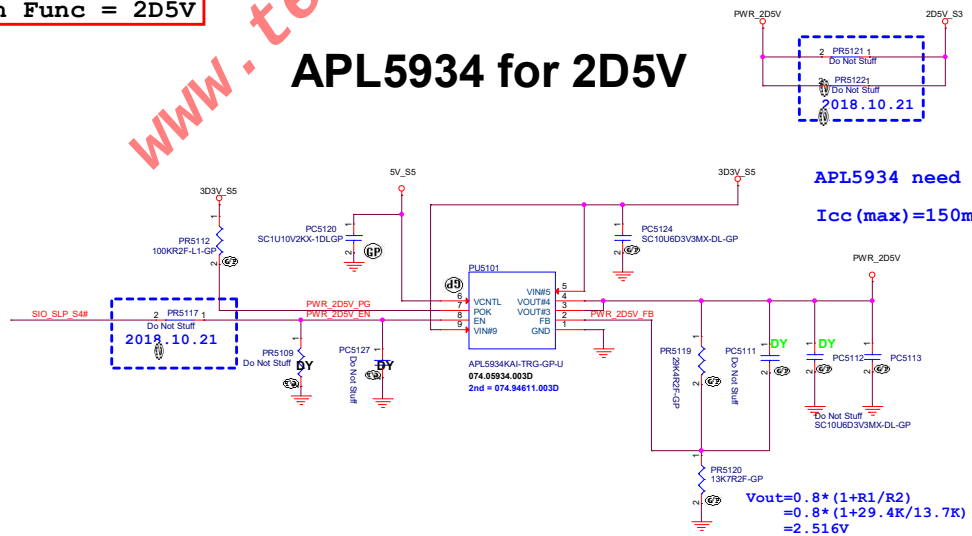
40 VDDQ_PWRGD
EE needs check it!!

5 SM_PGCNTL_Q

17,40,92 SIO_SLP_S4#

Main Func = 2D5V

APL5934 for 2D5V



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Title	Power_(5388_VDDQ/VTT)	
Size A2	Document Number Bolt WHL-U	Rev A00
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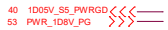
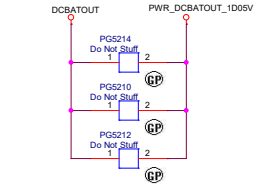
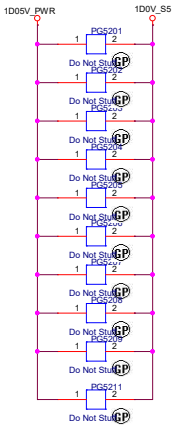
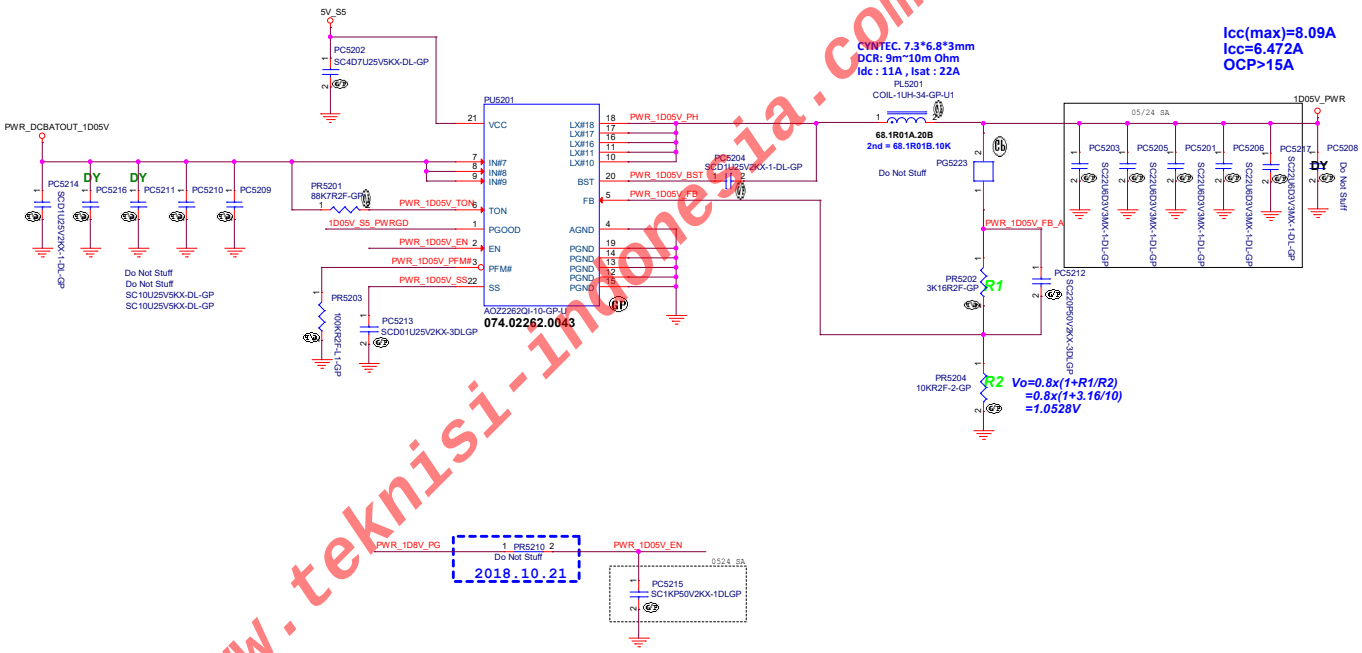
Main FUNC = PWR.Plane.Regulator_1D0V

AOZ2262 for 1D05V









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Title	AOZ2262_1D05V	
Size A2	Document Number BOLT WHL	Rev A00
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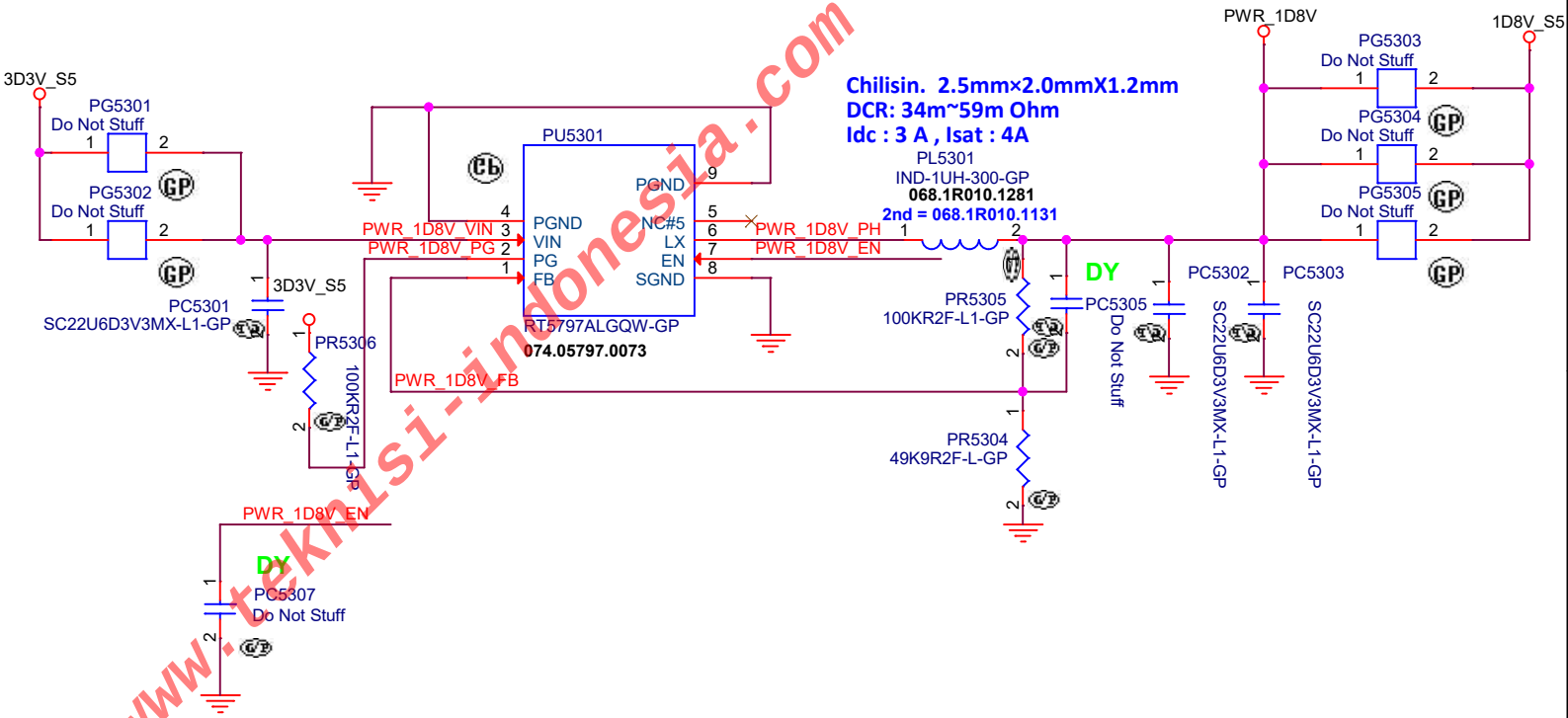
Main Func = 1D8V

52 PWR_1D8V_PG

25 3V_5V_DSW_OK

PR5308 2 1 PWR_1D8V_EN
Do Not Stuff
2018.10.21

Icc(max)=0.902A
Icc=0.632A
OCP>3A



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Title	1D8V	
Size A4	Document Number BOLT WHL	Rev A00
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Title: *(Reserved)*

Size	Document Number	Rev
Custom	BOLT WHL	A00

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Main Func = LCD

From CPU

4 eDP_TX_CPU_N0
4 eDP_TX_CPU_P0
4 eDP_TX_CPU_N1
4 eDP_TX_CPU_P1
4 eDP_AUX_CPU_P
4 eDP_AUX_CPU_N
4 EDP_HPD
4 EDP_VDD_EN
4 L_BKLT_CTRL

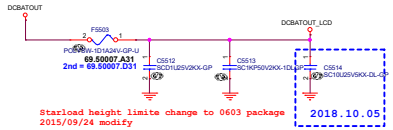
From EC

24 PANEL_BKEN
20,21 LCD_CBL_DET#
19 eDP_FHD_DET#

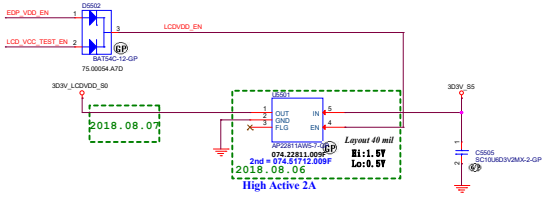
FOR TESTING

20 DBC_PANEL_EN
24 LCD_VCC_TEST_EN
24 LCD_TST
24 PANEL_MONITOR

INVERTER POWER

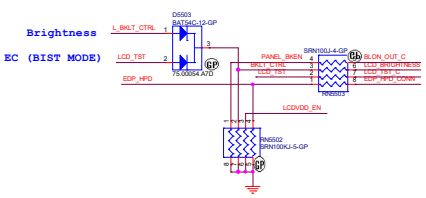


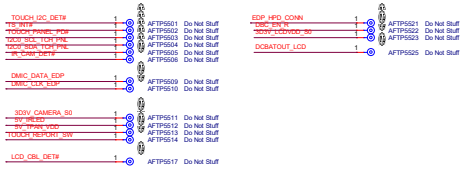
LCDVDD

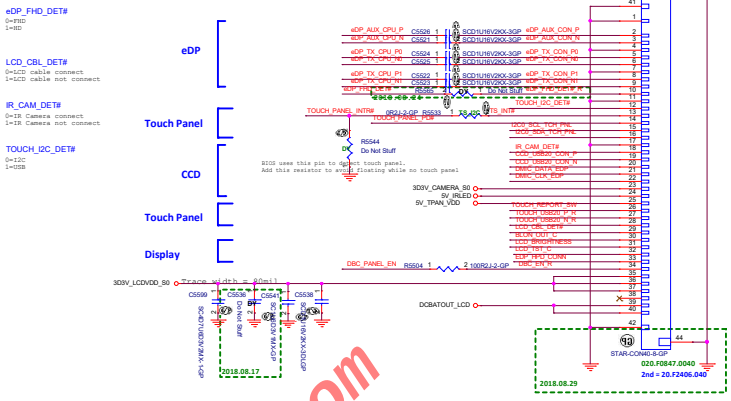


Brightness

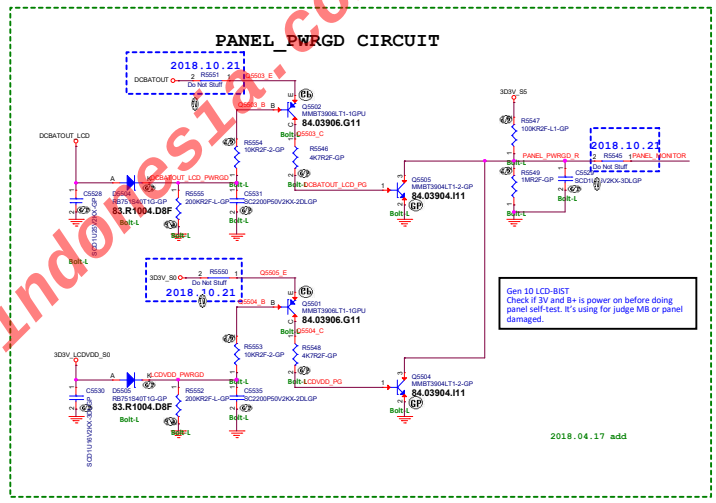
EC (BIST MODE)







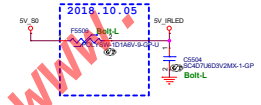
PANEL_PWRGD CIRCUIT

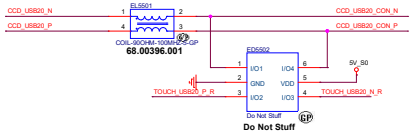


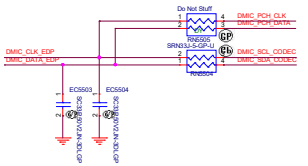
Main Func = CAMERA

20 IR_CAM_DET#
16 CCD_USB20_N
16 CCD_USB20_P
27 DMIC_SCL_CODEC
27 DMIC_SDA_CODEC
19 DMIC_PCH_CLK
19 DMIC_PCH_DATA

IR LED POWER



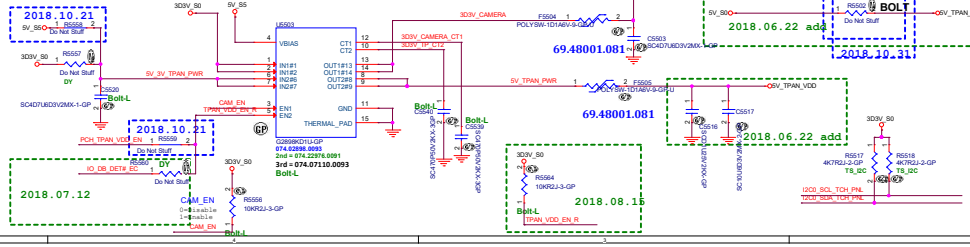


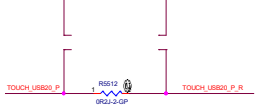


Main Func = Touch panel

20 I2C0_SCL_TCH_PNL
20 I2C0_SDA_TCH_PNL
16 TOUCH_USB20_N
16 TOUCH_USB20_P
3 TOUCH_PANEL_PDI#
3 TOUCH_PANEL_INTR#
24 TOUCH_REPORT_SW
24,66 IO_DB_DET#_EC
20 TOUCH_I2C_DET#
3 CAM_EN
20 PCH_TPAN_VDD_EN

TOUCH PANEL POWER





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Title: LCD&CAM&DMC&Touch
Size: Custom
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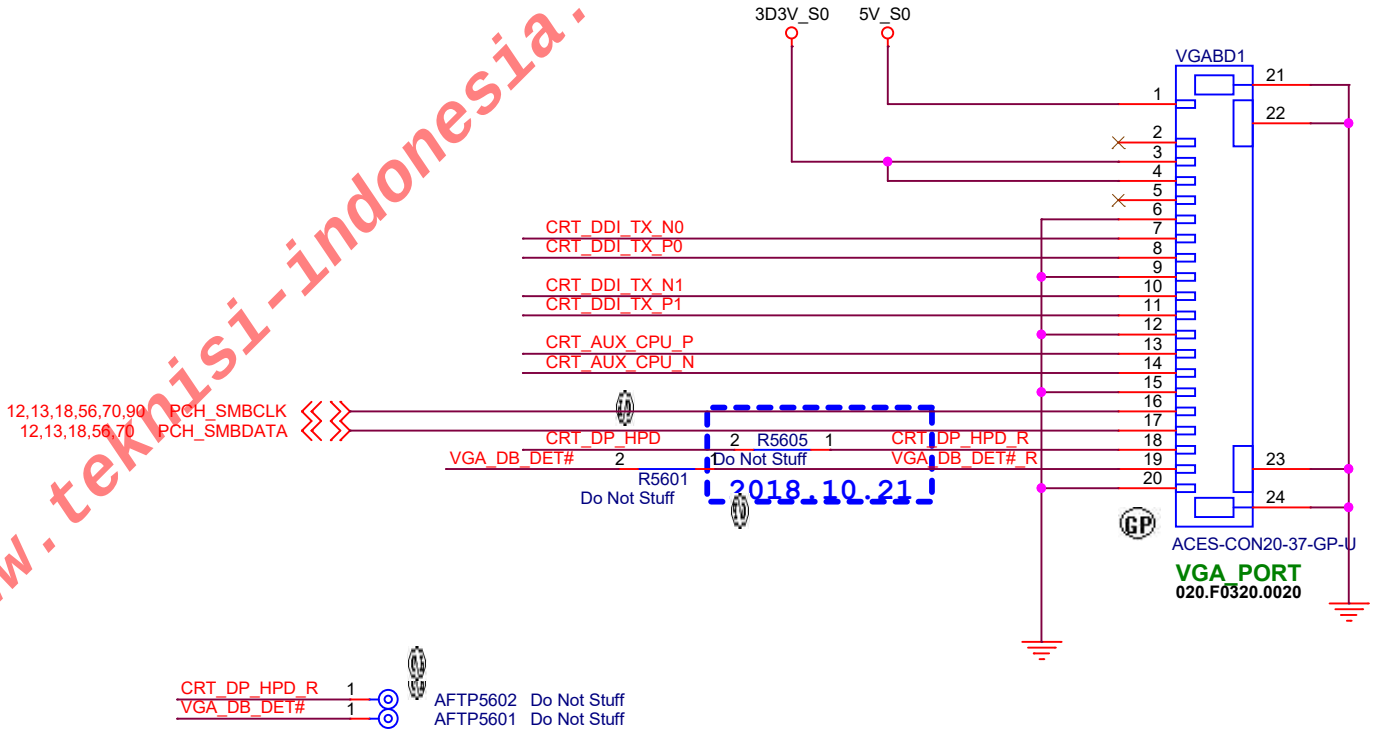
Main Func = CRT

58 CRT_DDI_TX_N0
58 CRT_DDI_TX_P0
58 CRT_DDI_TX_N1
58 CRT_DDI_TX_P1
58 CRT_AUX_CPU_P
58 CRT_AUX_CPU_N
12,13,18,56,70,90 PCH_SMBCLK
12,13,18,56,70 PCH_SMBDATA
58 CRT_DP_HPD
20 VGA_DB_DET#



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Title: CRT

Size	Document Number	Rev
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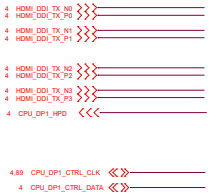
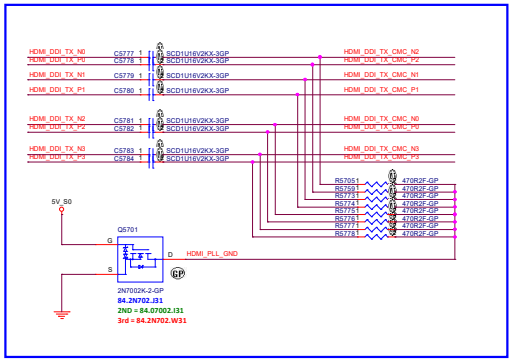
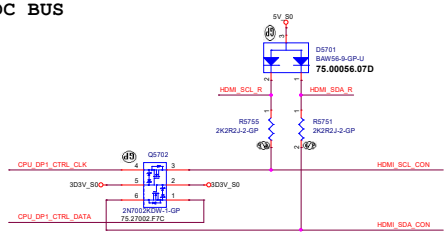
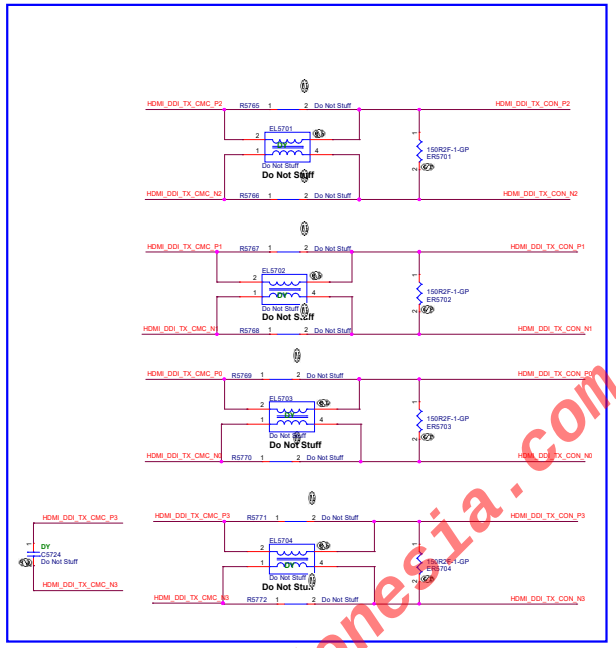
Main FUNC = HDMI

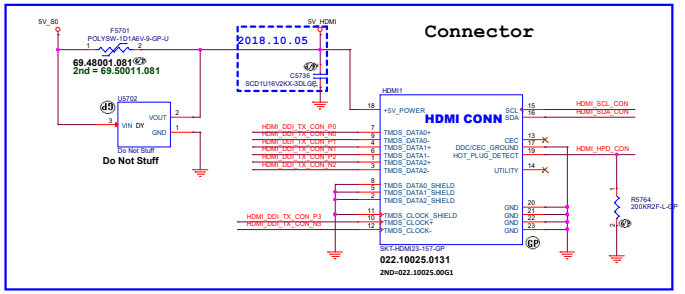




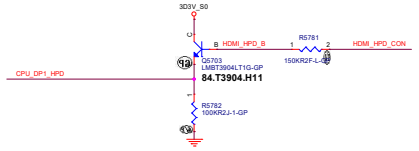
DDC BUS



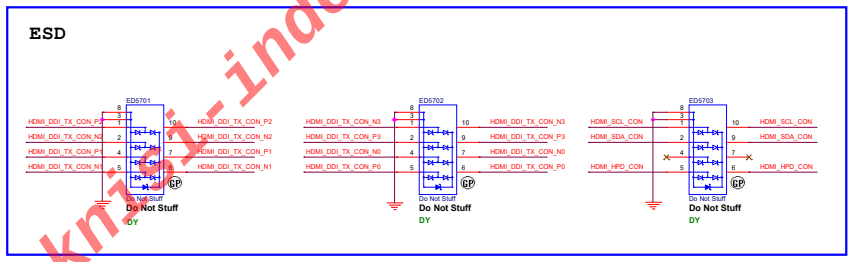




HOT PLUG



ESD



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Title: HDMI
Size: Document Number: BOLT WHL
Rev: A00
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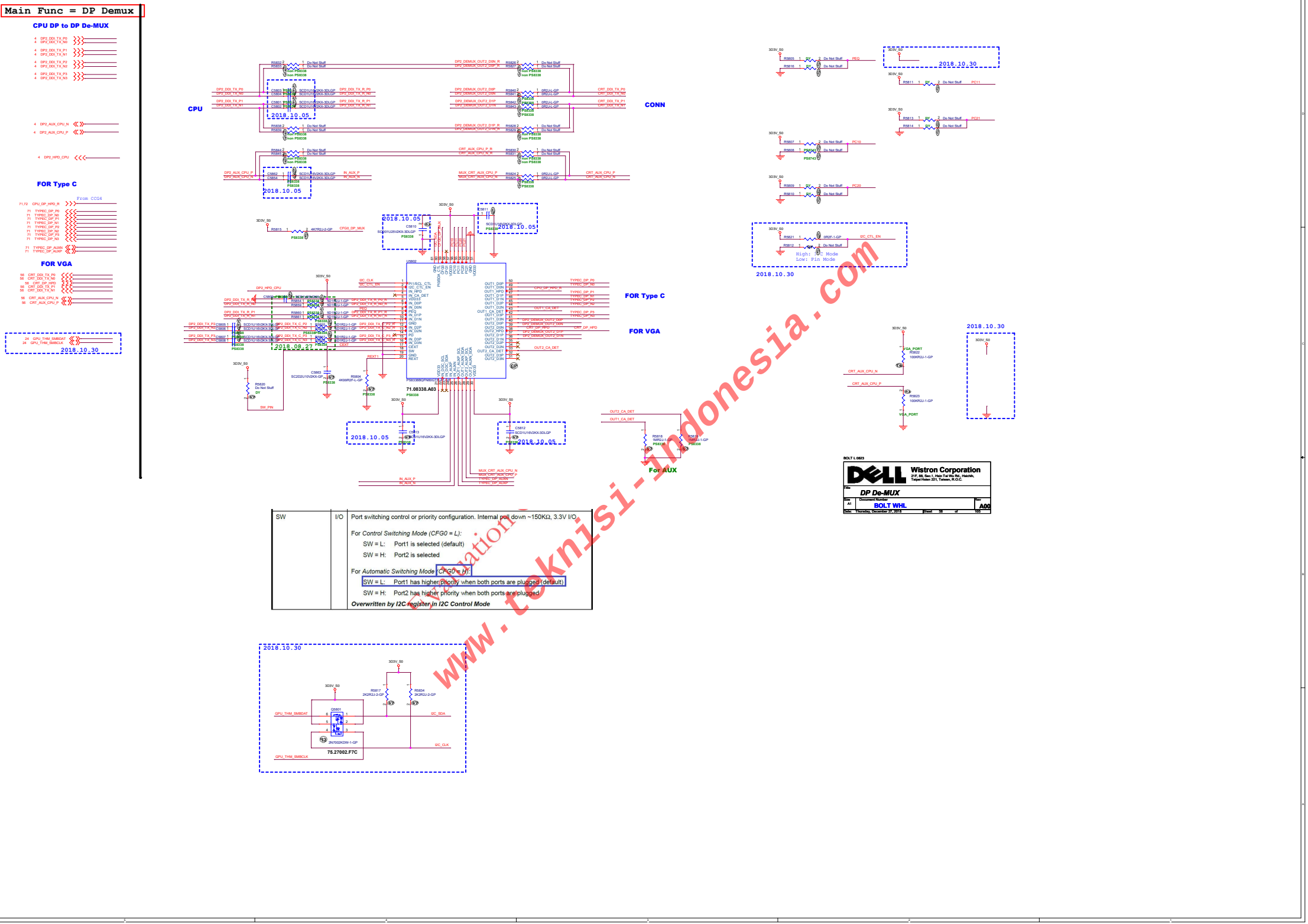
Main Func = DP Demux



(Blanking)

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Title: *(Reserved)*

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Main Func = HDD

HDD

16 HDD_SATA_TX_P11
16 HDD_SATA_TX_N11
16 HDD_SATA_RX_P11
16 HDD_SATA_RX_N11
70 FFS_INT2_Q
16 HDD_DEVSLP
18,20 HDD_DET#

SATA RE-DRIVER

2018.08.08

2018.10.05

HDD_SATA_TX_P11 C6028 SCD01U25V2KX-3DLGP HDD2_SATA_TX_CON_P
HDD_SATA_TX_N11 C6029 SCD01U25V2KX-3DLGP HDD2_SATA_TX_CON_N
HDD_SATA_RX_N11 C6030 SCD01U25V2KX-3DLGP HDD2_SATA_RX_CON_N
HDD_SATA_RX_P11 C6031 SCD01U25V2KX-3DLGP HDD2_SATA_RX_CON_P

HDD POWER

5V_S0
2018.10.21
80 mils
R6001 Do Not Stuff
5V_HDD_S0
C6008 SCF10U10V2MX-DL-GP-L HDD
C6007 SCD1U16V2KX-3DLGP HDD

SATA HDD Connector

HDD1
HDD_DET#
5V_HDD_S0
FFS_INT2_Q
5V_HDD_S0
HDD_Wire
HDD_DEVSLP
R6002 Do Not Stuff
HDD_DEVSLP_R
2018.10.21
HDD2_SATA_RX_CON_P
HDD2_SATA_RX_CON_N
HDD2_SATA_TX_CON_N
HDD2_SATA_TX_CON_P
020.F0320.0020
ACES-CON20-37-GP-U
2018.06.29
2ND=20.F2480.020

HDD2
HDD2_SATA_TX_CON_P
HDD2_SATA_TX_CON_N
HDD2_SATA_RX_CON_N
HDD2_SATA_RX_CON_P
HDD_DEVSLP_R
HDD_FFC
5V_HDD_S0
FFS_INT2_Q
2018.06.29
Do Not Stuff
Do Not Stuff
2ND = 020.K0158.0012

HDD ESD

Layout Note:
Place near HDD2
ED6001
Close to HDD1
HDD_SATA_TX_P11
HDD_SATA_TX_N11
HDD_SATA_RX_N11
HDD_SATA_RX_P11
Do Not Stuff
Do Not Stuff
DY
0628 change to commond part

Main Func = ODD

ODD

16 ODD_SATA_TX_N12
16 ODD_SATA_TX_P12
16 ODD_SATA_RX_P12
16 ODD_SATA_RX_N12
16 SATA1_ODD_PRSNT#

ODD Connector

5V_S0
R6003 Do Not Stuff
2018.10.21
5V_ODD_S0
C6018 Do Not Stuff ODD
C6019 Do Not Stuff ODD

ODD_SATA_TX_P12 Do Not Stuff C6014 ODD_SATA_TX_CON_P
ODD_SATA_RX_P12 Do Not Stuff C6011 ODD_SATA_RX_CON_P
SATA1_ODD_PRSNT# R6004 Do Not Stuff SATA_ODD_PRSNT#_R
ODD_S0
5V_ODD_S0
SATA_ODD_DA#_C
TP6001
ODD_SATA_TX_CON_N
ODD_SATA_RX_CON_N
C6013 Do Not Stuff ODD_SATA_TX_N12
C6010 Do Not Stuff ODD_SATA_RX_N12
Do Not Stuff
Do Not Stuff

ODD_SATA_TX_CON_P AFTP6001 Do Not Stuff
ODD_SATA_TX_CON_N AFTP6002 Do Not Stuff
ODD_SATA_RX_CON_N AFTP6003 Do Not Stuff
ODD_SATA_RX_CON_P AFTP6004 Do Not Stuff
SATA_ODD_PRSNT#_R AFTP6005 Do Not Stuff
5V_ODD_SU AFTP6006 Do Not Stuff

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Title: SATA IF_HDD/ODD
Size: A2
Document Number: BOLT WHL
Rev: A00
Date: Thursday, December 27, 2018
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Main FUNC = WLAN

BT

21 BLUETOOTH_EN
16 BT_USB20_N
16 BT_USB20_P

WLAN

18 CLK_PCIE_WLAN_REQ#
18 WLAN_CLK_CPU_N
18 WLAN_CLK_CPU_P
16 WLAN_PCIE_RX_N10
16 WLAN_PCIE_RX_P10
16 WLAN_PCIE_TX_N10
16 WLAN_PCIE_TX_P10

CNVI

19 BT_PCMFRM_RSTN
19 BT_PCMOUT_CLKREQ0
18 PULSAR_38P4M_REFCLK
20 CNV_RGI_RSP
15,20 CNV_RGI_DT_R
20 CNV_BRI_RSP
20 CNV_BRI_DT_R
21 CNV_WT_CLK_DP
21 CNV_WT_CLK_DN
21 CNV_WT_DP0
21 CNV_WT_DN0
21 CNV_WT_DP1
21 CNV_WT_DN1
21 CNV_WR_CLK_DP
21 CNV_WR_CLK_DN
21 CNV_WR_DP0
21 CNV_WR_DN0
21 CNV_WR_DP1
21 CNV_WR_DN1

Others

18,24 SUS_CLK
4 CNVI_EN#
17,24 AUX_EN_WOWL_R
17,18,24 JIO3_PCIE_WAKE#
21 WIFI_RF_EN
17,26,31,62,63,76,91 PLTRST#_CPU

CPU		WLAN
GPP_F8_RXD	COEX1	UART TXD
GPP_F9_TXD	COEX2	UART RXD
GPP_F0_BLANKING	COEX3	STANDARD PIN

3D3V_WLAN 1 AFTP6113
PLTRST#_CPU 1 AFTP6108
BLUETOOTH_EN 1 AFTP6112
WIFI_RF_EN 1 AFTP6110
CLK_PCIE_WLAN_REQ# 1 AFTP6109
BT_USB20_CON_N 1 AFTP6111
BT_USB20_CON_P 1 AFTP6114
JIO3_PCIE_WAKE# 1 FTP6115

R6125 1 CNVI 2 0R5J-5-GP
3D3V_S5
U6101
IN OUT
EN DY GND
OC#
C6102 SC4D7U6D3V3KX-L-GP
R6102 Do Not Stuff DY
Do Not Stuff
Do Not Stuff
2nd = 074.22811.009F
C6106 SCD1U25V2KX-1-DL-GP
C6105 SC10U6D3V3MX-DL-GP
3D3V_WLAN
3D3V_S0
R6124 non CNVI 2 Do Not Stuff
C6104 SCD1U16V2KX-3DLGP
2018.10.05
CNVI_EN# R6110 DY 1 Do Not Stuff
R6101 Do Not Stuff DY
CNVI_EN#_R
Q6102 DY
G D S
WLAN_EN#
AUX_EN_WOWL_R
Do Not Stuff
Do Not Stuff
2ND = 84.07002.I31
3rd = 84.07002.W31

3D3V_WLAN
WLAN1
PULSAR_38P4M_REFCLK
WIFI_RF_EN_R
BLUETOOTH_EN_R
PLTRST#_CPU
SUSCLR_WEAN
SUS_CLK R6117 1 33R2J-2-GP
2018.09.07
CNV_RGI_RSP R6120 1 22R2J-2-GP
CNV_BRI_DT_R
CNV_RGI_RSP_R
CNV_RGI_DT_R
CNV_BRI_RSP R6123 1 22R2J-2-GP
CNV_BRI_RSP_R
BT_PCMOUT_CLKREQ0
BT_PCMFRM_RSTN
3D3V_WLAN
R6121 DY 1 BT_PCMOUT_CLKREQ0
Do Not Stuff
R6122 2 1 BT_PCMFRM_RSTN
71K5R2F-1-GP
NP2
NGFF_KEY_E_75P
SKT-MINI67P-26-GP
062.10007.0511
NP1
WLAN_PCIE_TX_CON_N
WLAN_PCIE_TX_CON_P
C6107 SCD1U16V2KX-3DLGP
C6108 SCD1U16V2KX-3DLGP
RO13_20170822 C6107/C6108 move to C6107/C6108 close conn.
WLAN_PCIE_RX_N10
WLAN_PCIE_RX_P10
WLAN_PCIE_TX_N10
WLAN_PCIE_TX_P10
CNV_WT_CLK_DP
CNV_WT_CLK_DN
CNV_WT_DP0
CNV_WT_DN0
CNV_WT_DP1
CNV_WT_DN1
JIO3_PCIE_WAKE#
CLK_PCIE_WLAN_REQ#
WLAN_CLK_CPU_N
WLAN_CLK_CPU_P
CNV_WR_CLK_DP
CNV_WR_CLK_DN
CNV_WR_DP0
CNV_WR_DN0
CNV_WR_DP1
CNV_WR_DN1
BT_USB20_CON_N
BT_USB20_CON_P
R6105 1 2 Do Not Stuff
EL6101
Do Not Stuff
Do Not Stuff
DY
R6104 1 2 Do Not Stuff
BT_USB20_N
BT_USB20_P

3D3V_WLAN
R6114 10KR2J-3-GP
WIFI_RF_EN R6109 1 WIFI_RF_EN_R
0R2J-L-GP
BOLT-L
3D3V_WLAN
R6115 10KR2J-3-GP
BLUETOOTH_EN R6108 1 BLUETOOTH_EN_R
0R2J-L-GP
BOLT-L

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Title: NGFF_WLAN CONN
Size: A2
Document Number: BOLT WHL
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Main FUNC = WWAN

19,21,24 WWAN_DB_DET#

24 INT#_ITE8010
24 CLK_ITE8010
24 DAT_ITE8010

WWAN

16 WWAN_PCIE_RX_N
16 WWAN_PCIE_RX_P
16 WWAN_PCIE_TX_N
16 WWAN_PCIE_TX_P

18 WWAN_CLKREQ_CPU_N
18 WWAN_PCIE_CLK_P
18 WWAN_PCIE_CLK_N

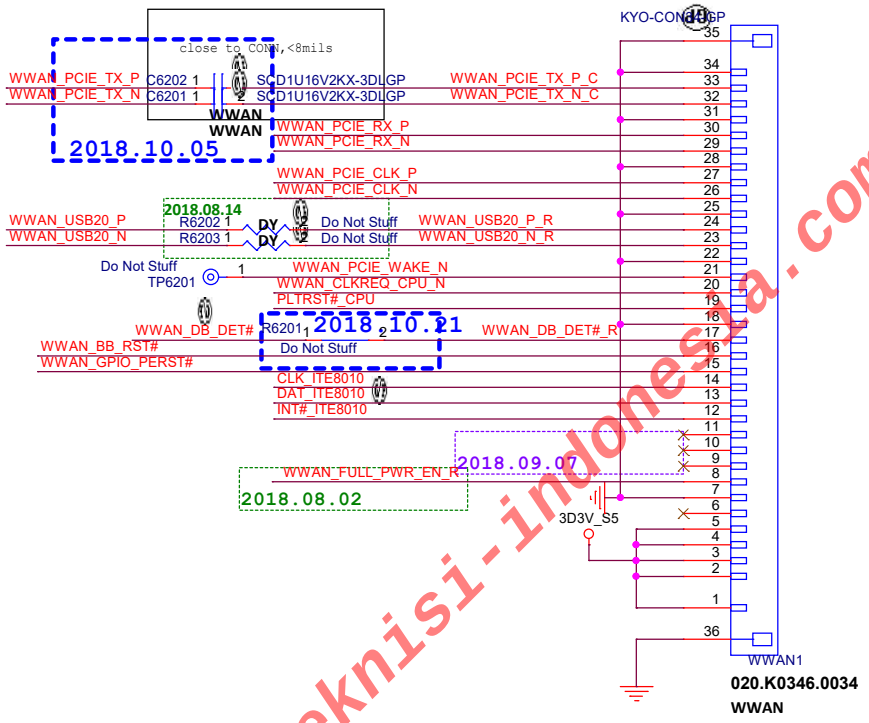
16 WWAN_USB20_N
16 WWAN_USB20_P

17,26,31,61,63,76,91 PLTRST#_CPU

WWAN_FULL_PWR_EN_R 20

WWAN_BB_RST# 21

WWAN_GPIO_PERST# 20



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Title: WWAN

Size	Document Number	Rev
Custom	BOLT WHL	A00

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Main Func = M.2 SSD

M.2 PCIE/SATA FOR BOLT

16 SSD_PCIE_TX_P16
16 SSD_PCIE_TX_N16
16 SSD_PCIE_RX_N16
16 SSD_PCIE_RX_P16

16 SSD_PCIE_TX_P15
16 SSD_PCIE_TX_N15
16 SSD_PCIE_RX_P15
16 SSD_PCIE_RX_N15

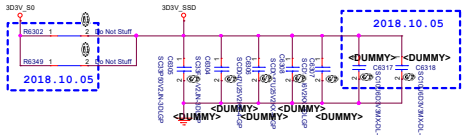
16 SSD_PCIE_TX_P14
16 SSD_PCIE_TX_N14
16 SSD_PCIE_RX_P14
16 SSD_PCIE_RX_N14

16 SSD_PCIE_TX_P13
16 SSD_PCIE_TX_N13
16 SSD_PCIE_RX_P13
16 SSD_PCIE_RX_N13

18 SSD_CLK_CPU_P_4
18 SSD_CLK_CPU_N_4
18 CLK_PCIE_NVME_REQ#

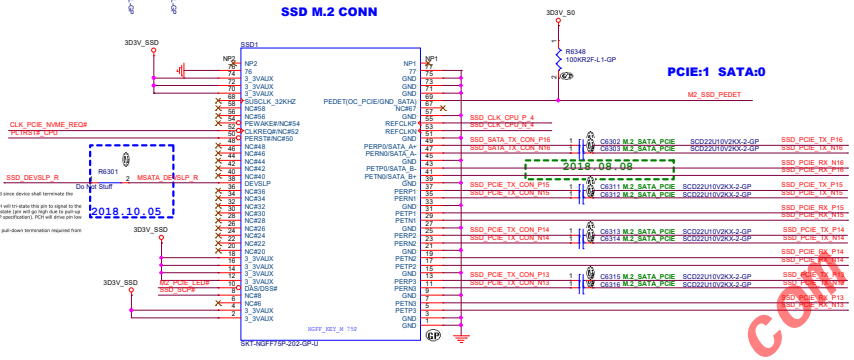
5,31,61,62,76,91 PLTRST# CPU
16 M2_SSD_PEDET

16 SSD_DEVSLP_R
64 M2_PCIE_LED#
24 SSD_SCI#



2018.08.02

SSD M.2 CONN



2018.08.07

Important! SATA Host DEVSLP signals shall not be terminated since device shall terminate the signal.

- This is an open-drain pin on the PCH side. PCH will tri-state this pin to signal to the SATA device that it may enter a lower power state (pin will go high due to pull-up that's internal to the SATA device, per DEVSLP specification). PCH will drive pin low to wake or when exiting from DEVSLP.
- When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (OD)(3.3V)	PEDET (I2C PCIe/GND-SATA)	69
66	SUS_STAT# (OD)(3.3V)	N/C	67
	Connector Key	Connector Key	
56	N/C	CLKREQ#	57
54	PEWAKE# (I/OD)(3.3V) or N/C	REFCLKp	55
52	CLKREQ# (I/OD)(3.3V) or N/C	GND	53
50	PERST# (I)(3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS#(I/O)(3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1
	Connector Key	Connector Key	

Table 13-11. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF[2]	None	None[3]

Notes:

1. Design Constraint: For PCIe only application, refer to the PCIe guidelines for details.
2. Design Constraint: For SATA only application, both Tx and Rx channels need to have 10 nF capacitors on the motherboard. This option supports all SATA devices. However, the Rx 10 nF capacitor can be removed if DC coupled ODDs / devices are NOT used.
3. Design Constraint: For PCIe* Gen 2/ SATA multiplexed configuration, motherboard Tx requires a 100 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
4. Design Constraint: For PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**
5. Design Constraints, Required: Refer to the Chapter 3, "General Differential Signals Design Guidelines" along with the additional guidelines in this section for all design optimization guidelines.
6. Design Constraint: For PCIe* lane that needs to support either **PCIe* Gen2 devices** or **PCIe* Gen3 devices**, follow the PCIe* Gen 3/ SATA multiplexed configuration, motherboard Tx requires a 220 nF AC capacitor and NO AC capacitor is required for motherboard Rx channel. **This option DOES NOT support DC coupled ODDs / Devices.**

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Title: *mSATA*

Size: Custom | Document Number: BOLT WHL | Rev: A00

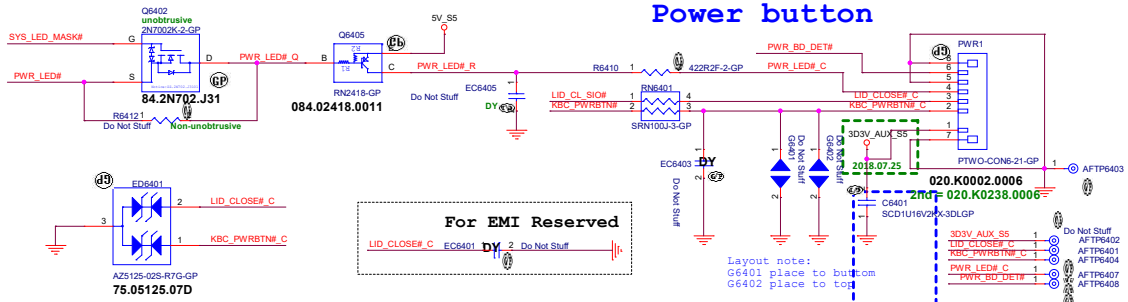
Date: Thursday, December 27, 2018 | Sheet 63 of 105

Main Func = Power BTN

24 PWR_LED#
20,21 PWR_BD_DET#
24,92 LID_CL_SIO#
24,92 KBC_PWRBTN#

NONE FINGER PRINT 才會上件

Power button

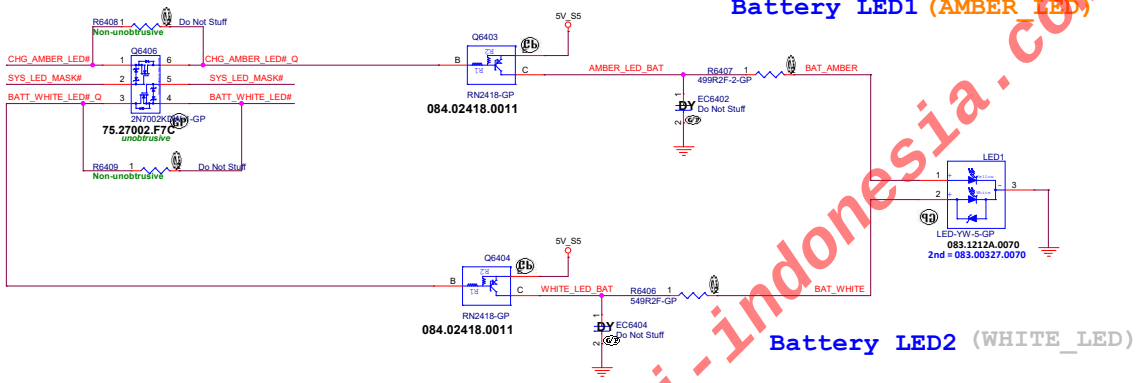


Main Func = Battery LED

Low actived from KBC GPIO

24,32 SYS_LED_MASK#
24 CHG_AMBER_LED#
24 BATT_WHITE_LED#

Battery LED1 (AMBER_LED)

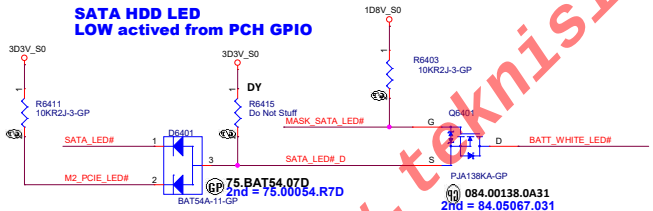


Battery LED2 (WHITE_LED)

Main Func = HDD LED

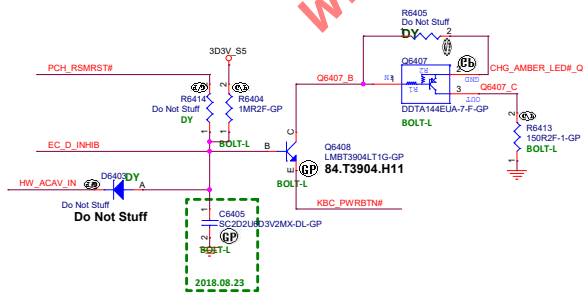
24 MASK_SATA_LED#
16 SATA_LED#
63 M2_PCIE_LED#

SATA HDD LED
LOW actived from PCH GPIO



Main Func = M-BIST

17,24 PCH_RSMRST#
24 EC_D_INHIB
24,43,44 HW_ACAV_IN



M-BIST(Mainboard Built-In Self Test)Check if MB is damage while press power button. There is a LED will light up to indicate the MB is damage by

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Title: LED Board&Power Button
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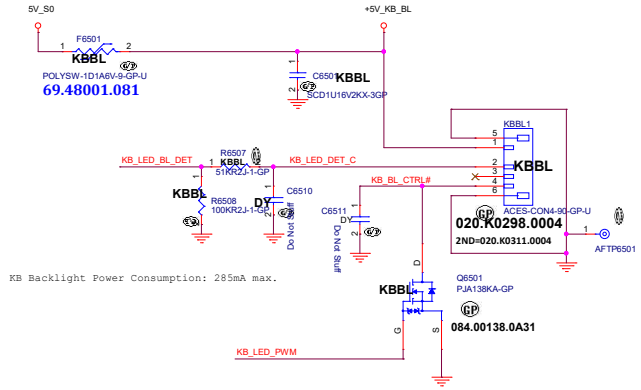
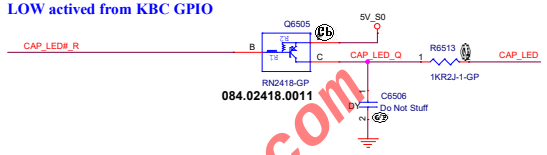
Main Func = KB

24 CAP_LED#_R
24 KSI[0..7]
24 KSO[0..16]
20 KB_DET#
19 KB_LED_BL_DET
24 KB_LED_PWM

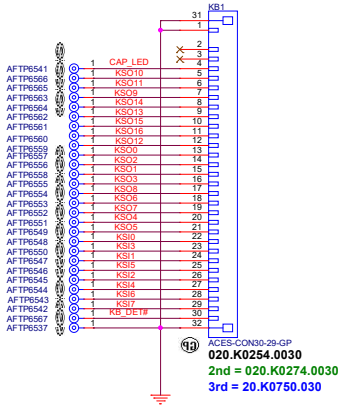
Keyboard Backlight (Reserved)



CAP LED Control
LOW actived from KBC GPIO

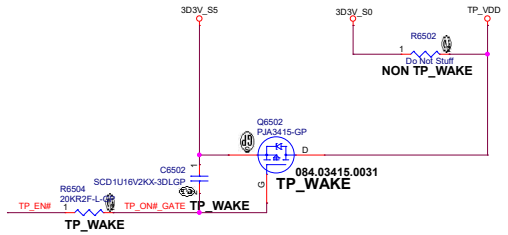


Internal Keyboard Connector

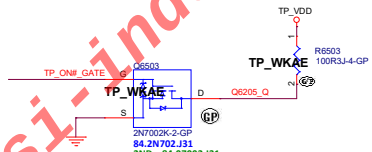


Main Func = TPAD

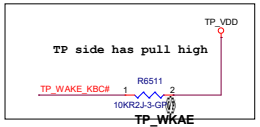
24 TP_EN#
24 CLK_TP_SIO
24 DAT_TP_SIO
20 I2C0_SCL_TCH_PAD
20 I2C0_SDA_TCH_PAD
3,24 TP_WAKE_KBC#
24 PTP_DIS#



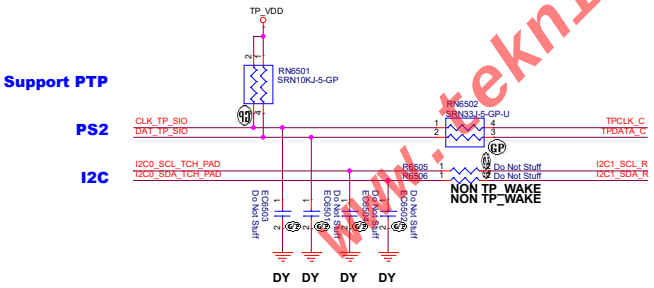
TP_VDD Discharge Circuit

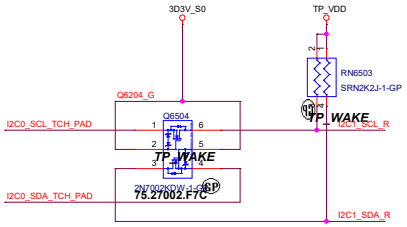


Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

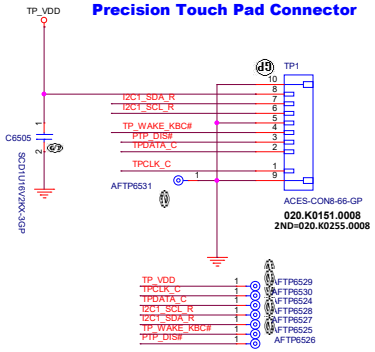


Support PTP





Precision Touch Pad Connector



Pin number	Pin name
1	VDD
2	DAT(I2C)
3	CLK(I2C)
4	GND
5	ATTN
6	GPIO
7	DAT(PS2)
8	CLK(PS2)

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Title: Key Board&Touch Pad

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Main Func = IO Connector

USB 2.0

16 USB2_USB20_N
16 USB2_USB20_P

16 CARD1_USB20_N
16 CARD1_USB20_P

21 IO_DB_DET#

19 IO_DB_DET#_GPPG5

20 SD_READ_MODE#

24,55 IO_DB_DET#_EC

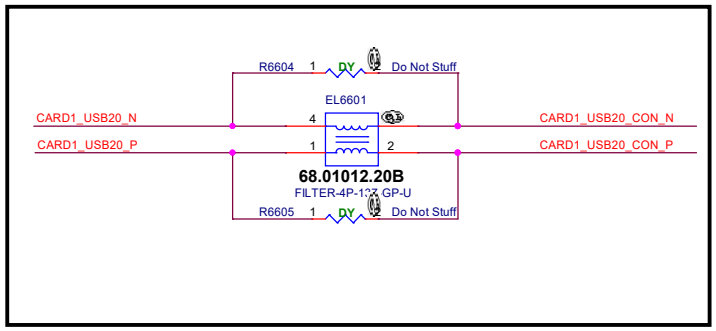
USB OC

16 USB_OC1#

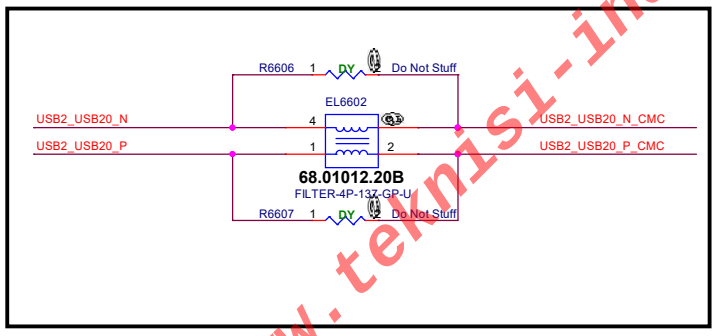
USB Switch Enable

24,35 USB_EN#

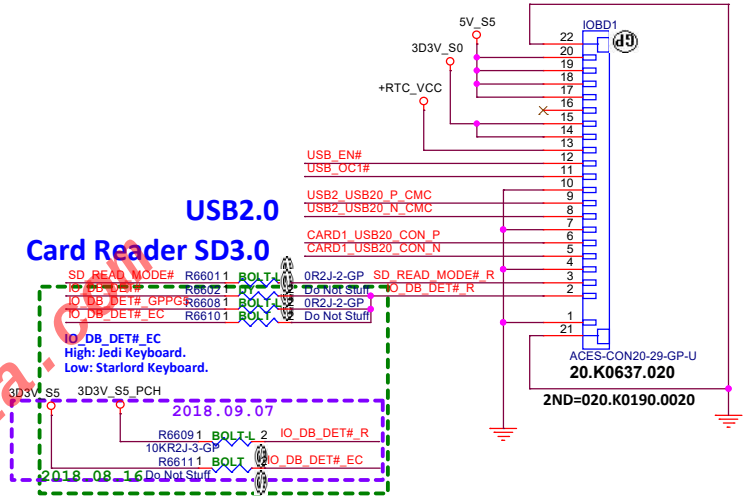
USB2.0 CARD

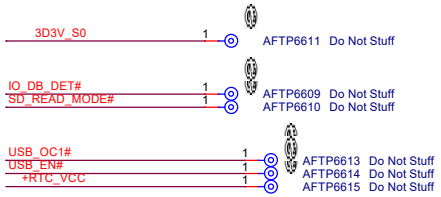


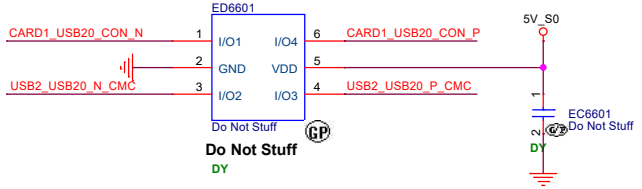
USB2.0 CARD



USB2.0 Card Reader SD3.0







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Title: *IO Board Connector*

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Title

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Main Func = Debug

18,24 ESPI_CLK
18,24 ESPI_RESET#
18,24 ESPI_CS#

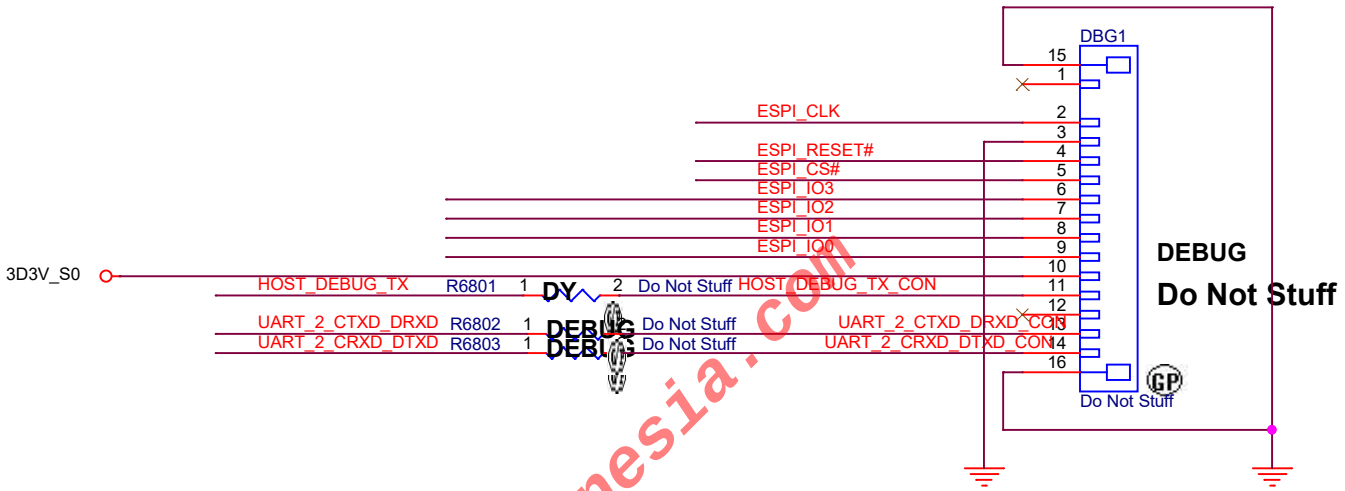
24 HOST_DEBUG_TX

20 UART_2_CTXD_DRXD
20 UART_2_CRXD_DTXD

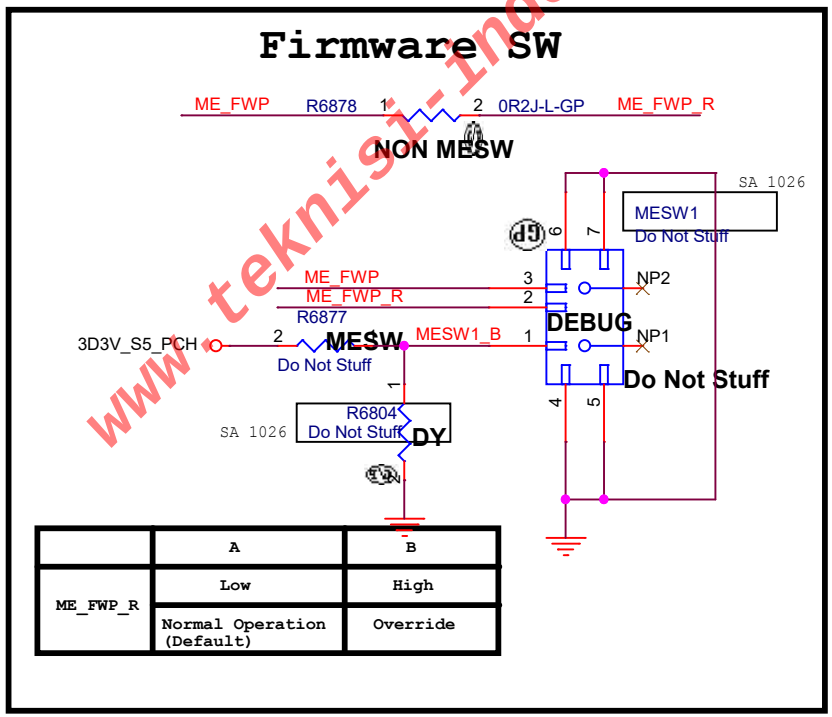
18,24 ESPI_IO[3..0]
ESPI_IO3
ESPI_IO1
ESPI_IO2
ESPI_IO0

24 ME_FWP
19 ME_FWP_R

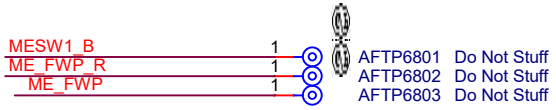
Debug Connector



Firmware SW



	A	B
ME_FWP_R	Low	High
	Normal Operation (Default)	Override



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Title: *Dubug connector*

Size	Document Number	Rev
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Title

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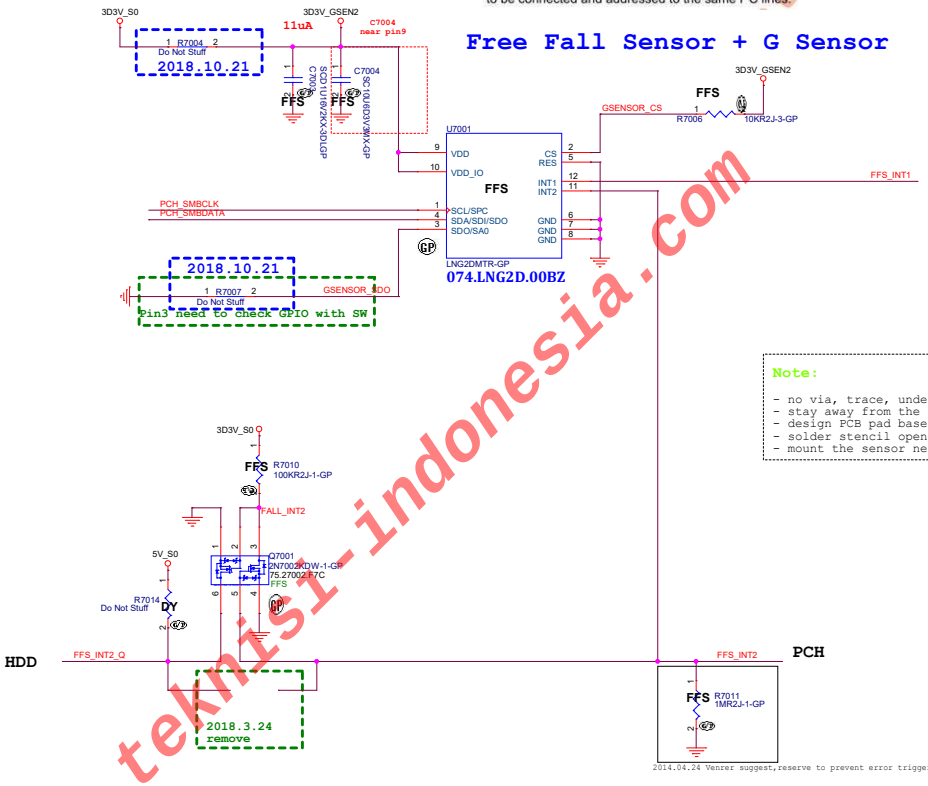
Main Func = Free Fall Sensor

12,13,18,56 PCH_SMBDATA
12,13,18,56,90 PCH_SMBCLK

18 FFS_INT1
20 FFS_INT2
60 FFS_INT2_Q

The slave address (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Free Fall Sensor + G Sensor



Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

Note:

(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

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Main FUNC = TYPEC MUX

From USB HOST

From DP Demux

From CCG4

From CCG4 to MUX & DP Demux

To Type-C CONNECTOR

From EC

To Type-C CONNECTOR

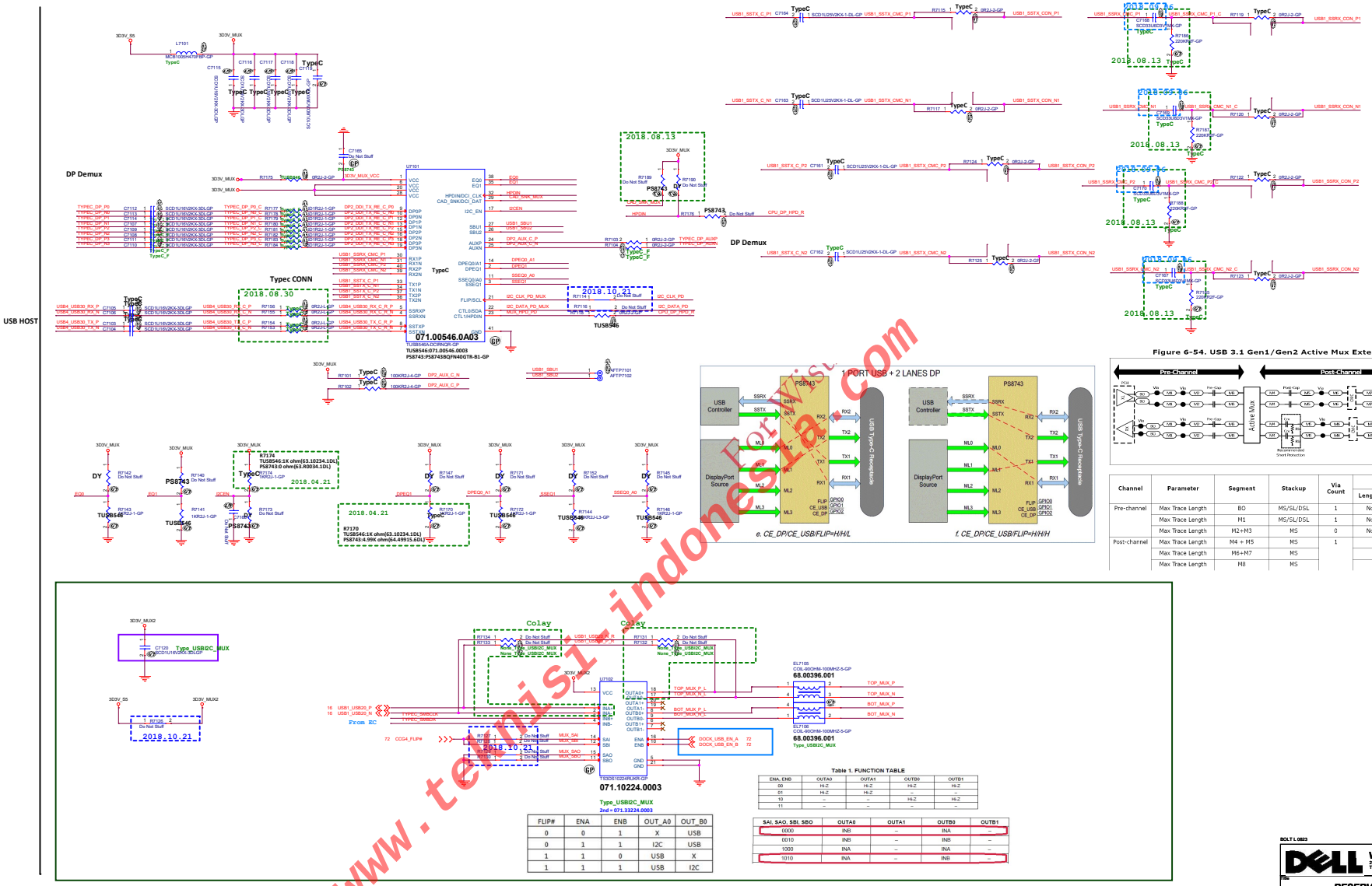

Figure 6-54. USB 3.1 Gen1/Gen2 Active Mux External Topology

Channel	Parameter	Segment	Stackup	Via Count	Gen2	
					Length (mm)	Length (mils)
Pre-channel	Max Trace Length	B0	MS/SL/DSL	1	Note#1*	Note#1*
	Max Trace Length	M1	MS/SL/DSL	1	Note#1*	Note#1*
	Max Trace Length	M2+M3	MS	0	Note#1*	Note#1*
Post-channel	Max Trace Length	M4 + M5	MS	1	7.6	300
	Max Trace Length	M6+M7	MS		7.6	300
	Max Trace Length	M8	MS		10.2	400

Table 1. FUNCTION TABLE

ENA, ENB	OUTA0	OUTA1	OUTB0	OUTB1
00	Hi-Z	Hi-Z	Hi-Z	Hi-Z
01	Hi-Z	Hi-Z	–	–
10	–	–	Hi-Z	Hi-Z
11	–	–	–	–

FLIP#	ENA	ENB	OUT_A0	OUT_B0
0	0	1	X	USB
0	1	1	I2C	USB
1	1	0	USB	X
1	1	1	USB	I2C

SAI, SAO, SBI, SBO	OUTA0	OUTA1	OUTB0	OUTB1
0000	INB	–	INA	–
0010	INB	–	INB	–
1000	INA	–	INA	–
1010	INA	–	INB	–

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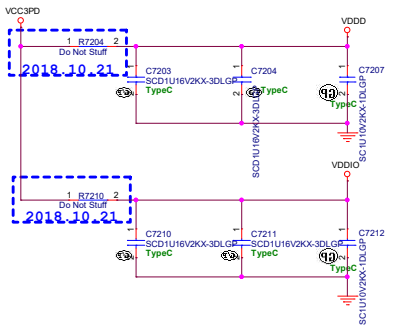
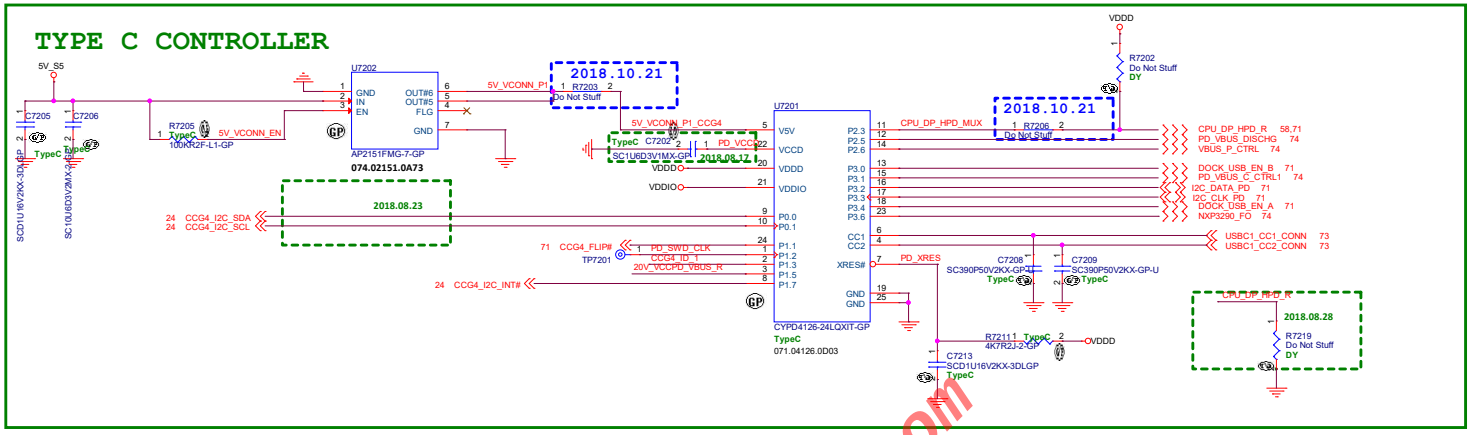
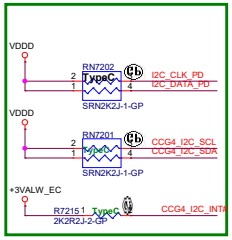
Main FUNC = CONTROLLER

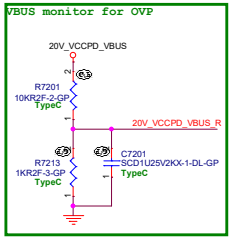
Power

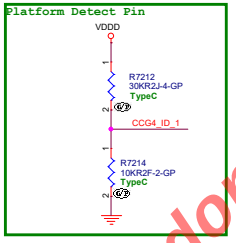


TYPE C CONTROLLER





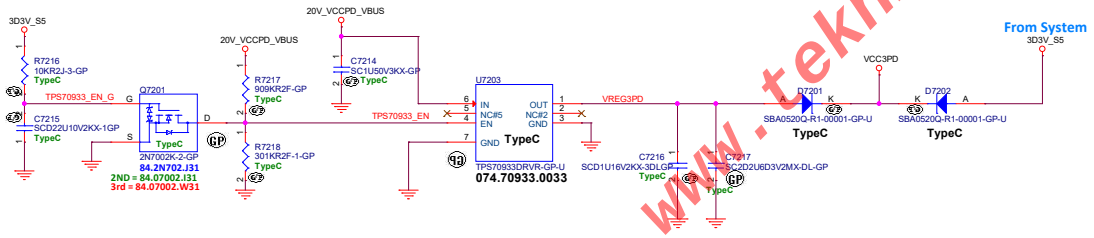




	CCG4_ID_1	R7212	R7214	計算值	理論值
0/8	L0	DY	64.10035.6DL (100K)	0	0
1/8	L1	064.71535.06D1 (715K)	64.10035.6DL (100K)	0.123	0.125
2/8	L2	64.30035.6DL (300K)	64.10035.6DL (100K)	0.25	0.25
3/8	L3	64.20035.6DL (200K)	64.12035.6DL (120K)	0.375	0.375
4/8	L4	64.10035.6DL (100K)	64.10035.6DL (100K)	0.5	0.5
5/8	L5	64.12035.6DL (120K)	64.20035.6DL (200K)	0.625	0.625
6/8	L6	64.22035.6DL (220K)	64.59035.6DL (590K)	0.728	0.75
7/8	L7	64.10035.6DL (100K)	064.71535.06D1 (715K)	0.877	0.875

S.No	Project Name	ODM	CCG4_ID_1	Single/ Dual Port	Port 1 Configuration	Port 2 Configuration	Voltage level	Voltage value
1	Bolt (WHL) Data Only with PS8743B Mux	Wistron	L0	Single	USB	N/A	**L0**	0V
2	Bolt (WHL) Data Only with TUSB546 Mux	Wistron	L1	Single	USB	N/A	**L1**	3.3V/8
3	Bolt (CNL) Data Only with PS8743B Mux	Wistron	L2	Single	USB	N/A	**L2**	2 * 3.3V/8
4	Bolt (CNL) Data Only with TUSB546 Mux	Wistron	L3	Single	USB	N/A	**L3**	3 * 3.3V/8
5	Bolt (WHL) Full Feature with PS8743B Mux	Wistron	L4	Single	USB+DP+ PD Charging	N/A	**L4**	4 * 3.3V/8
6	Bolt (WHL) Full Feature with TUSB546 Mux	Wistron	L5	Single	USB+DP+ PD Charging	N/A	**L5**	5 * 3.3V/8
7	Bolt (CNL) Full Feature with PS8743B Mux	Wistron	L6	Single	USB+DP+ PD Charging	N/A	**L6**	6 * 3.3V/8
8	Bolt (CNL) Full Feature with TUSB546 Mux	Wistron	L7	Single	USB+DP+ PD Charging	N/A	**L7**	7 * 3.3V/8

For Dead Battery modify



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Title: **USB3.0 PORT**

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Main FUNC = TYPEC CONNECTOR

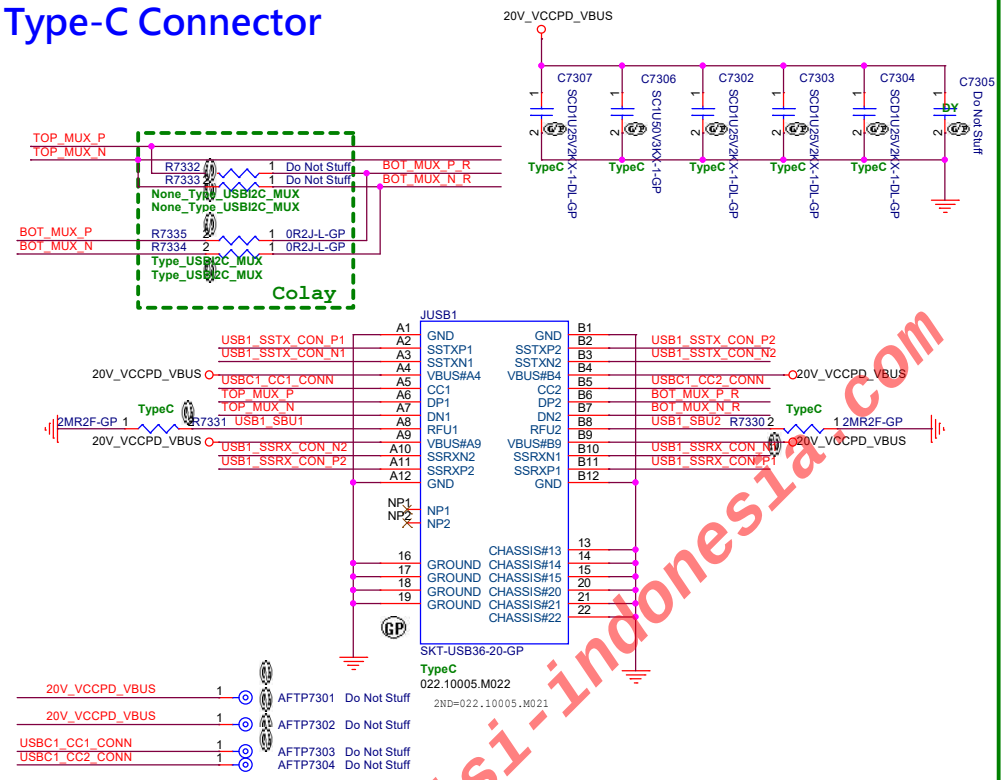
71 USB1_SSRX_CON_N1
71 USB1_SSRX_CON_P1
71 USB1_SSRX_CON_N2
71 USB1_SSRX_CON_P2
71 USB1_SSTX_CON_N1
71 USB1_SSTX_CON_P1
71 USB1_SSTX_CON_N2
71 USB1_SSTX_CON_P2

71 USB1_SBU1
71 USB1_SBU2
72 USBC1_CC1_CONN
72 USBC1_CC2_CONN

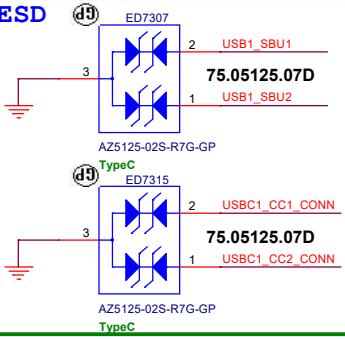
From USB2.0/ I2C Mux

71 TOP_MUX_P
71 TOP_MUX_N
71 BOT_MUX_P
71 BOT_MUX_N

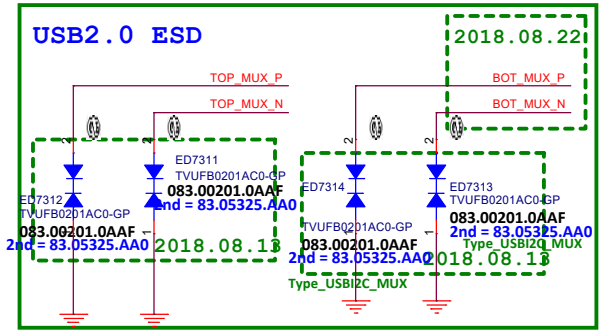
Type-C Connector



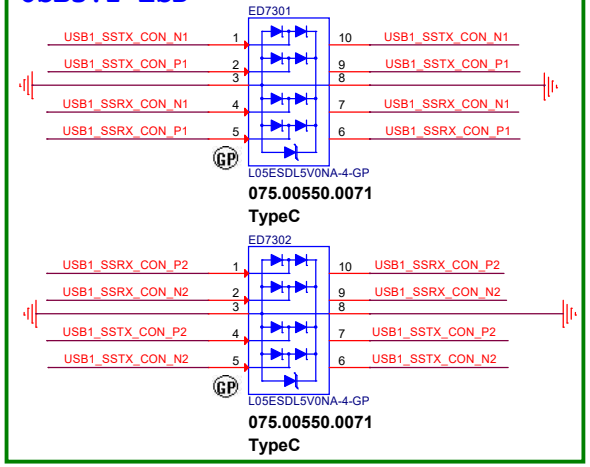
CC & SBU ESD



USB2.0 ESD



USB3.1 ESD



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Title: GPU(1/5)PEG

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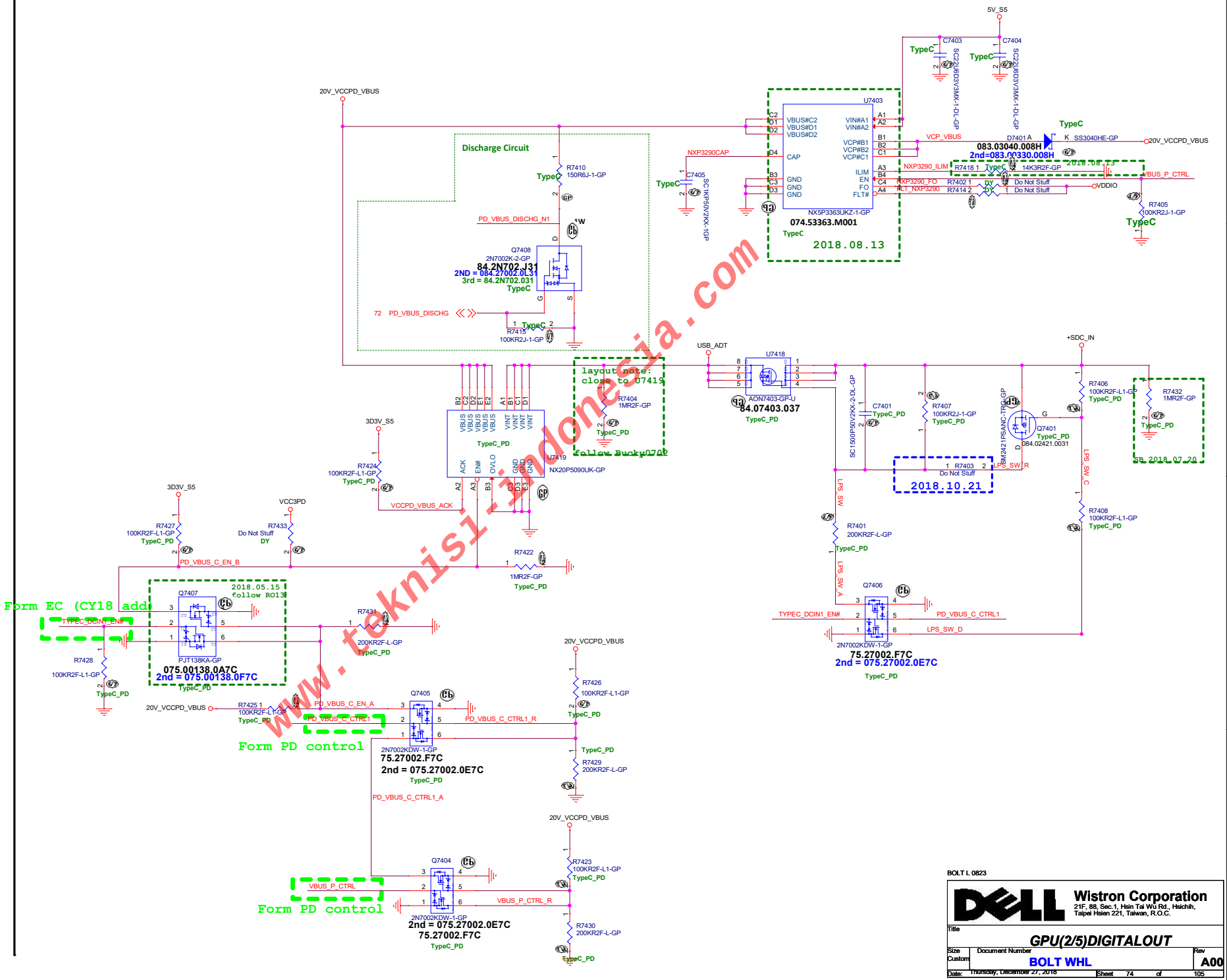
Main FUNC = LPS

72 PD_VBUS_C_CTRL1
72,74 VBUS_P_CTRL
24 TYPEC_DCIN1_EN#
72 NXP3290_FO
72,74 VBUS_P_CTRL

44 VCCPD_VBUS_ACK



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Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
Custom	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 74 of 105

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Title: GPU(3/5)VRAMI/F

Size	Document Number	Rev
A3	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 75 of 106

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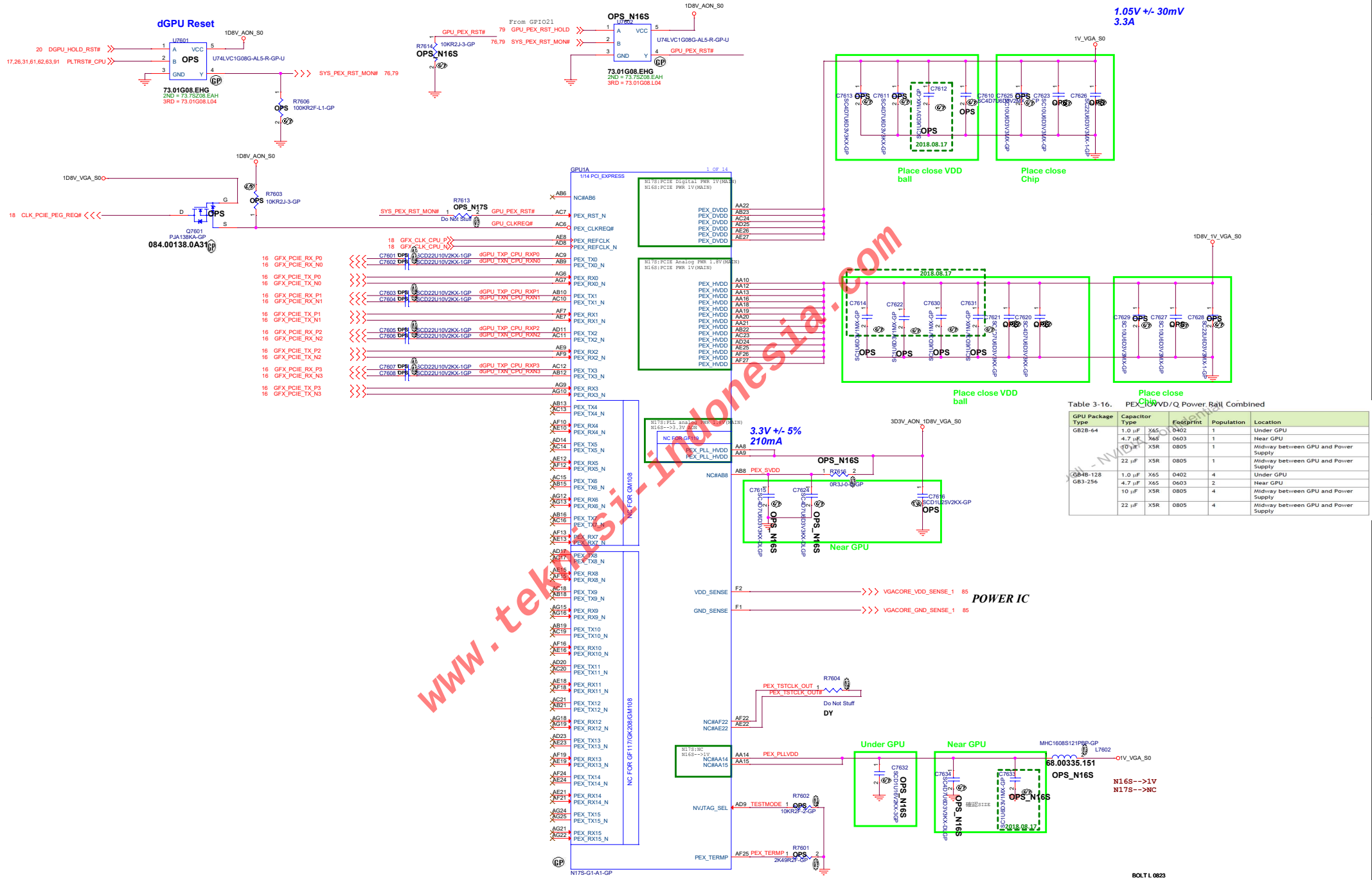

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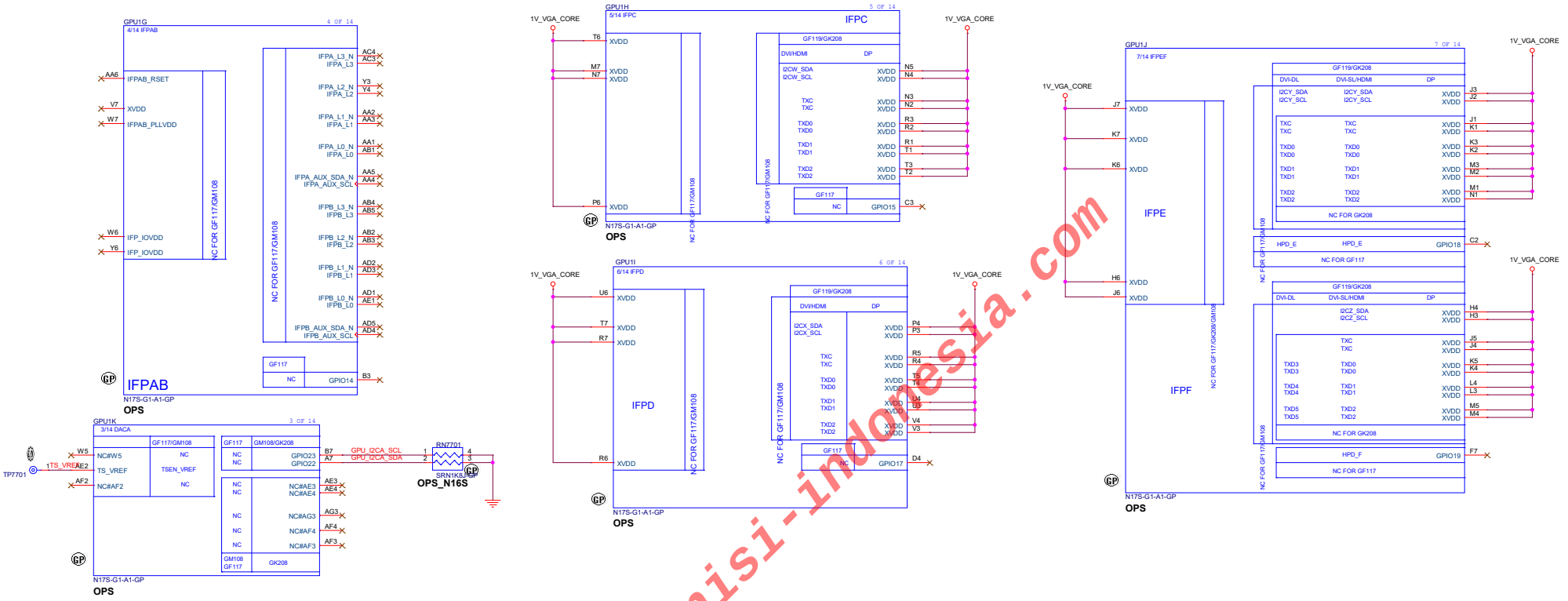

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Title: GPU(2/5)DIGITALOUT

Size	Document Number	Rev
A2	BOLT WHL	A00

Date: Thursday, December 27, 2018 Sheet 77 of 105

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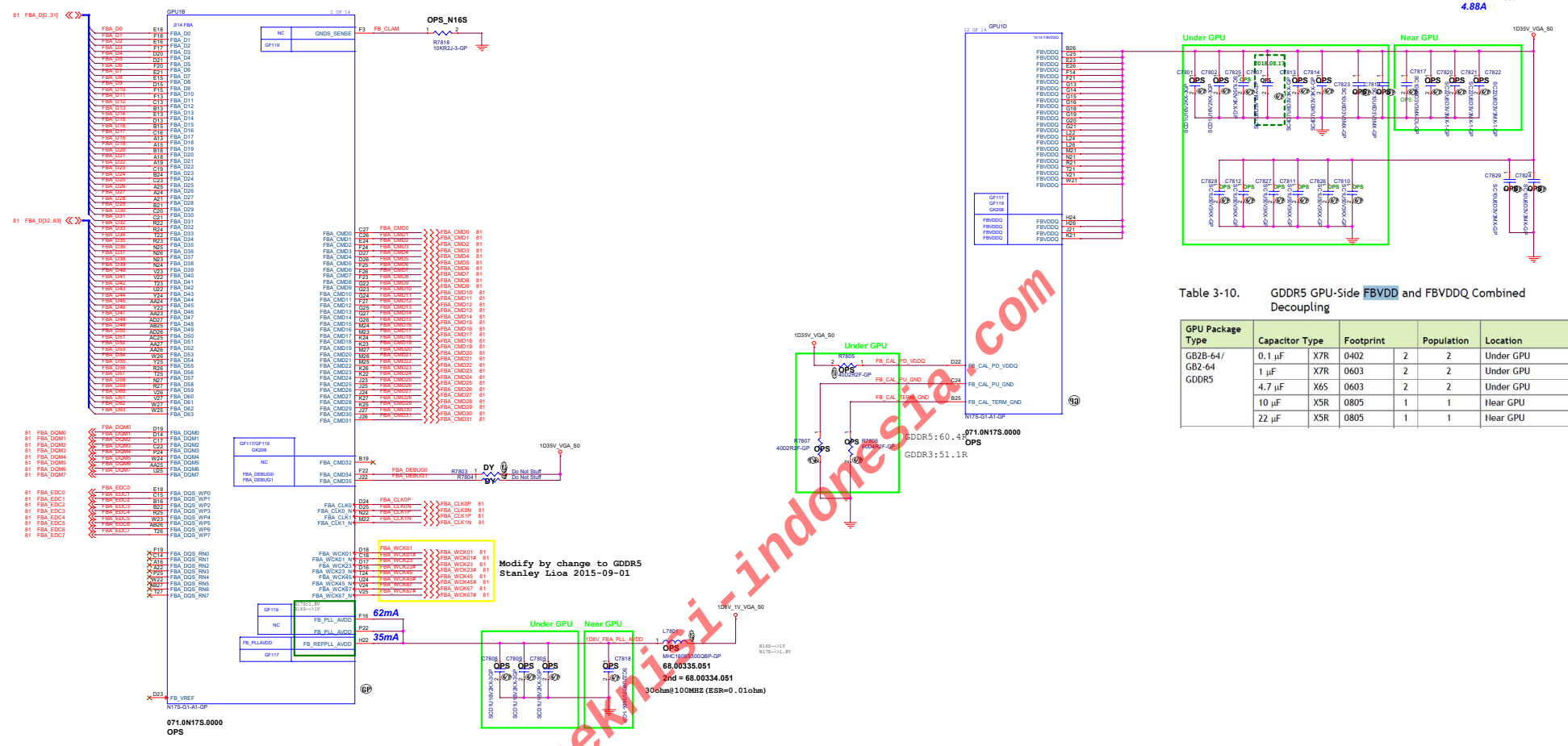

Note:
Reference NV-DDR5 CRB and DOH70 by GDDR5

Table 3-10. GDDR5 GPU-Side FBVDD and FBVDDQ Combined Decoupling

GPU Package Type	Capacitor Type		Footprint	Population		Location
GB2B-64/ GB2-64 GDDR5	0.1 µF	X7R	0402	2	2	Under GPU
	1 µF	X7R	0603	2	2	Under GPU
	4.7 µF	X6S	0603	2	2	Under GPU
	10 µF	X5R	0805	1	1	Near GPU
	22 µF	X5R	0805	1	1	Near GPU

Table 3-37. GPCPLL_AVDD0/1, LXS_PLLVDD, and FB_PLL_DLL_AVDD0/1 Power Rail Filter Combined

GPU Package	PLL Rails	Capacitor Type		Footprint	Population	Location
GB3B-256	GPCPLL_AVDD0/1 + LXS_PLLVDD + FB_PLL_DLL_AVDD0/1	0.1 µF	X7R	0402	5	Under GPU
		22 µF	X5R	0805	1	Near GPU
		Bead Type				
		30 Ω (ESR=0.010 Ω)		0603	1	Near GPU

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Title: GPU(3/5)VRAM/F
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Date: Thursday, December 27, 2018 | Sheet 78 of 105

Main Func = dGPU

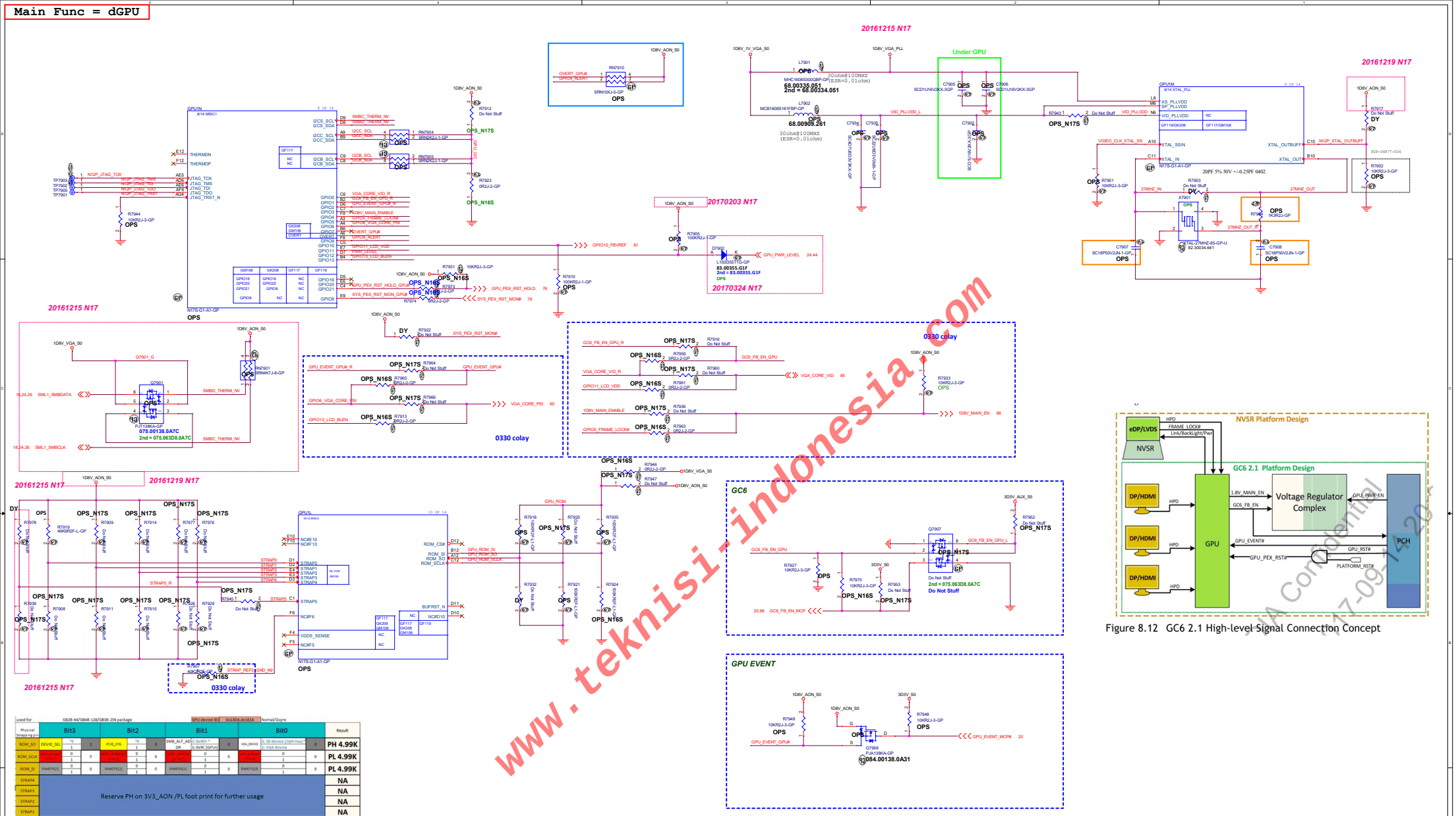

Figure 8.12 GC6 2.1 High-level Signal Connection Concept

Bit3	Bit2	Bit1	Bit0	Result
ROM_SO DEVID_SEL	PCIE_CFG	SMB_ALT_AD DIS	VGA_DEVICE	PH 4.99K
ROM_SCLK				PL 4.99K
ROM_SI RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	PL 4.99K
STRAP4				NA
STRAP3	Reserve PH on 3V3_AON /PL foot print for further usage			NA
STRAP2				NA
STRAP1				NA
STRAP0	Pull up 49.9 KΩ to 3V3_AON and reserve Pull down resister foot print.			PH49.9K

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Memory Date Code Minimum	Status
			Hynix	H5GQ8H24MJR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
			Micron	MT51J256M32HF-70:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-80:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x8	3000	N/A	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x8	3000	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x9	3000	N/A	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x9	3000	N/A	Substitution allowed with waiver[2]

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade (MHz)	Date Code Minimum	Status
			Samsung	K4G80325FB-HC25	B-die	0x0	3250	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-T2C	M-die	0x5	2500	N/A	Post production ready
			Hynix	H5GC8H24AJR-R0C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Hynix	H5GQ8H24AJR-R4C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-60:A	A-die	0x1	2500	N/A	Production ready
			Micron	MT51J256M32HF-70:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-80:A	A-die	0x1	3000	N/A	Substitution allowed with waiver[2]
			Micron	MT51J256M32HF-70:B	B-die	0x8	3000	N/A	Post production ready
			Micron	MT51J256M32HF-80:B	B-die	0x8	3000	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-R0C	A-die	0x9	3000	N/A	Post production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0x9	3000	N/A	Substitution allowed with waiver[2]
			Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Samsung	K4G80325FB-HC28	B-die	0x0	3000	N/A	Substitution allowed with waiver[2]
		512Mx16	Samsung	K4G80325FB-HC25	B-die	0x0	3250	N/A	Substitution allowed with waiver[2]
			Hynix	H5GC8H24AJR-T2C	M-die	0x5	2500	N/A	Post production ready
			Hynix	H5GC8H24AJR-R0C	M-die	0x5	3000	N/A	Substitution allowed with waiver[2]

N16S	ROM_SO	ROM_SCLK	ROM_SI	STRAP5	STRAP4	STRAP3	STRAP2	STRAP1	STRAP0
HYNIX-IC H5GC8H24AJR-R0C FBGA170P	H(4.99K)	L(4.99K)	H(10K)	NC	NA	NA	NA	NA	H(49.9K)
SAMSUNG- K4G80325FB-HC28 FBGA170P	H(4.99K)	L(4.99K)	L(4.99K)	NC	NA	NA	NA	NA	H(49.9K)
MICRON-MT51J256M32HF-70:B FBGA170P	H(4.99K)	L(4.99K)	H(4.99K)	NC	NA	NA	NA	NA	H(49.9K)

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Title: GPU(4/5)GPIO/STRAP

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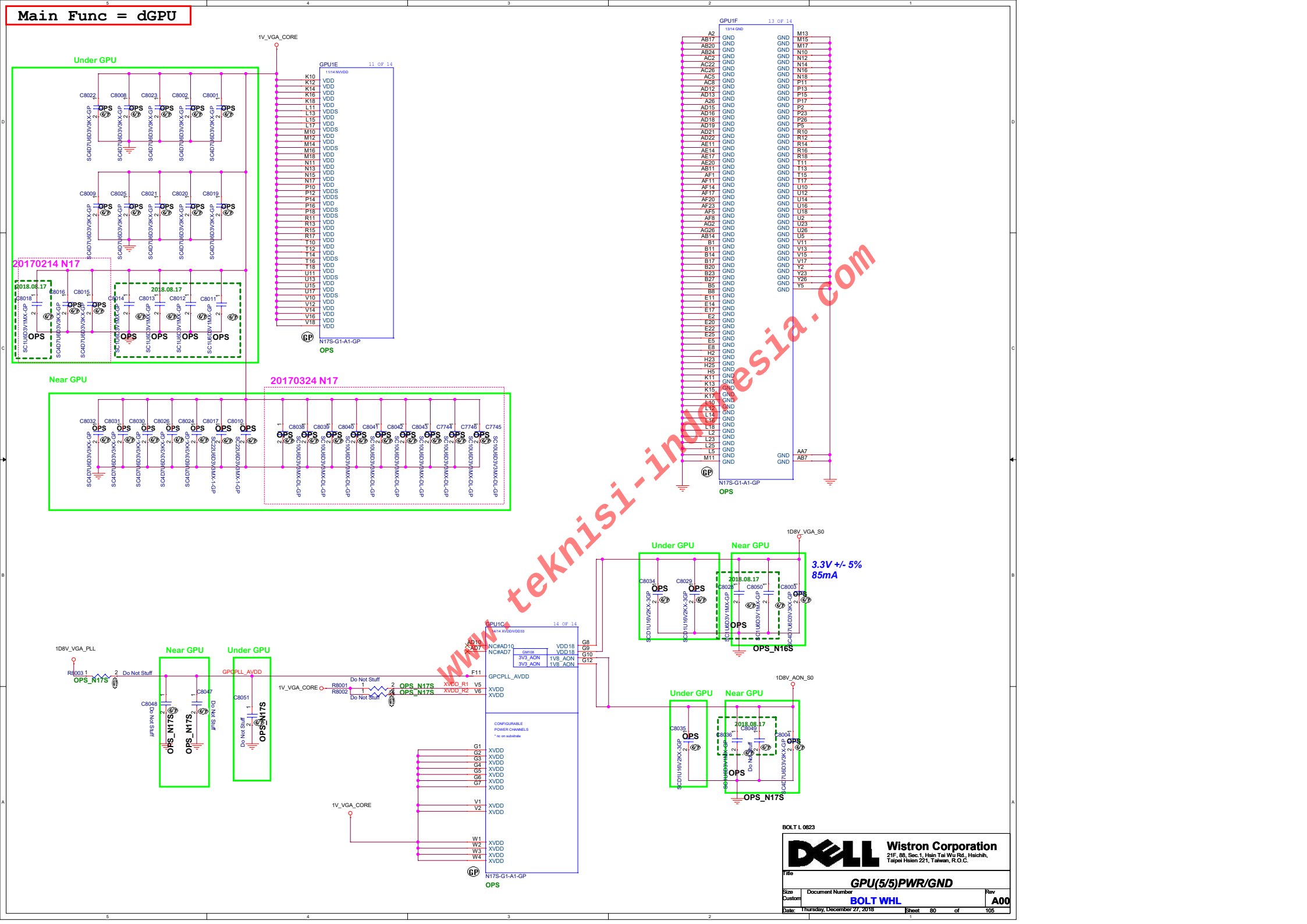

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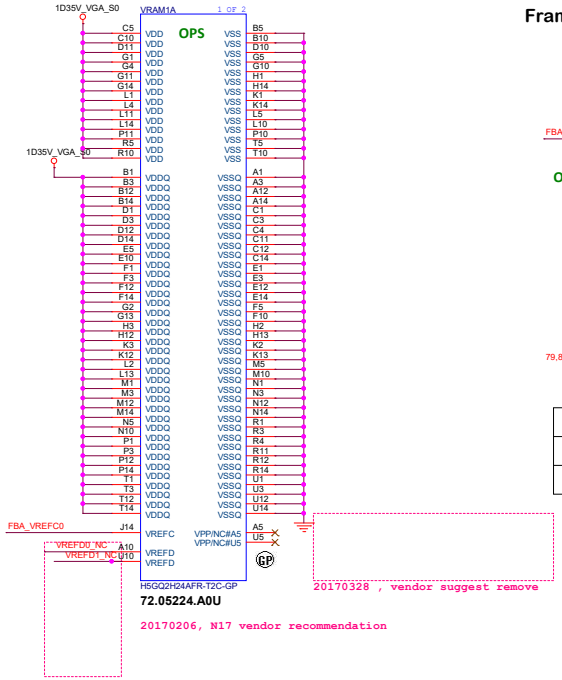
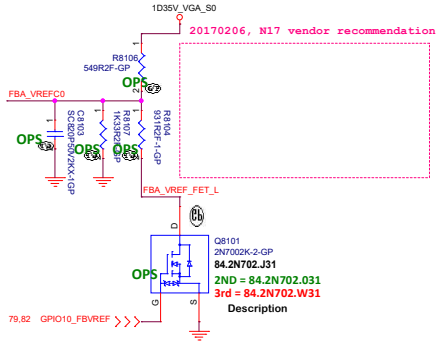
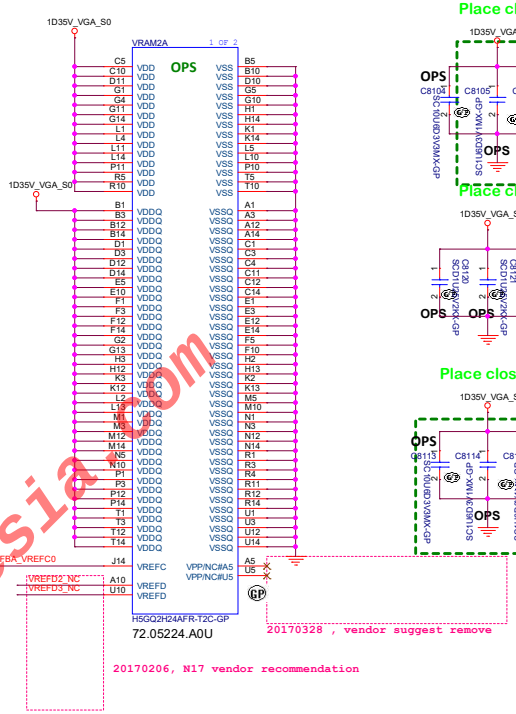


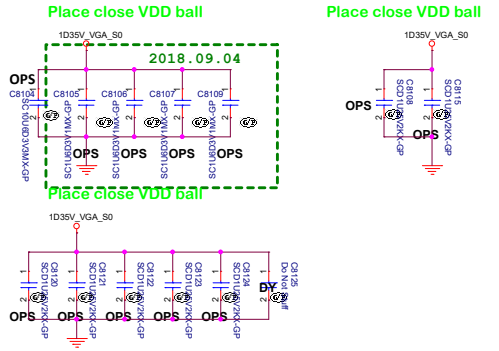
Frame Buffer Patition A-Lower Half

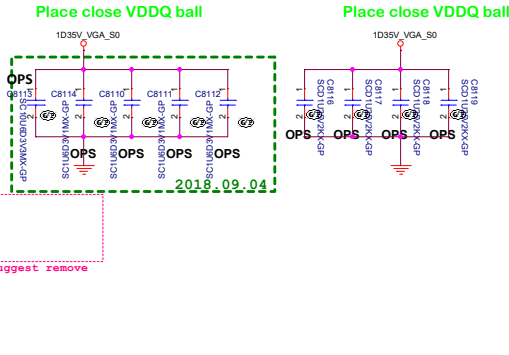


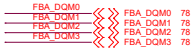
FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low









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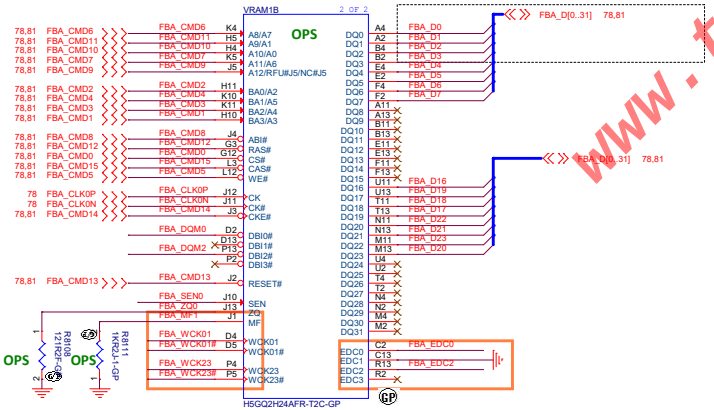

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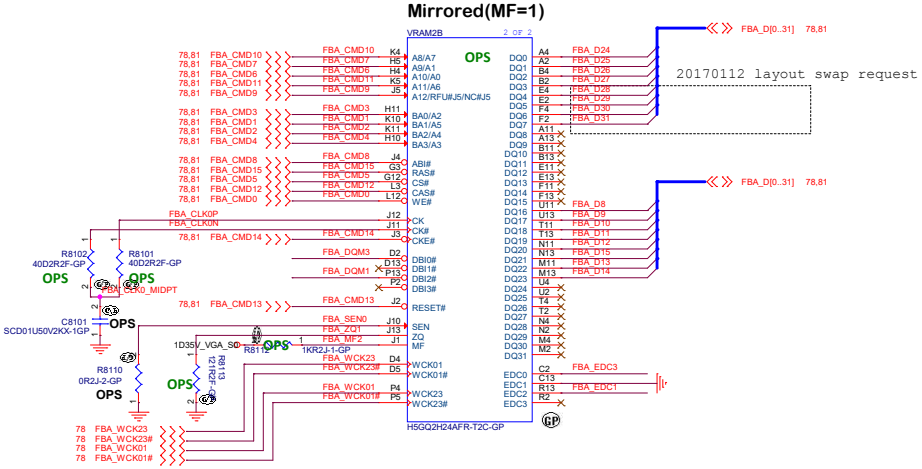

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Title: GPU-VRAM1,2 (1/4)

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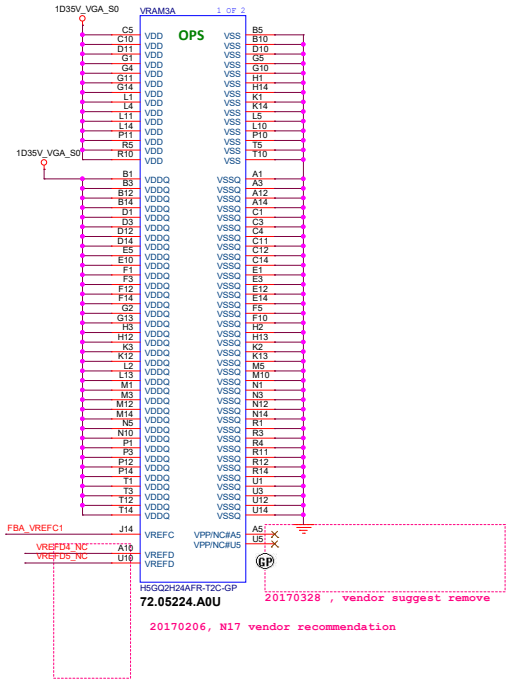
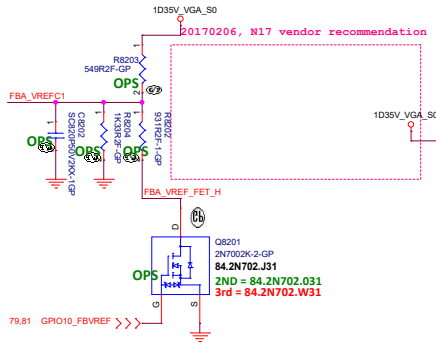
Main FUNC = VRAM

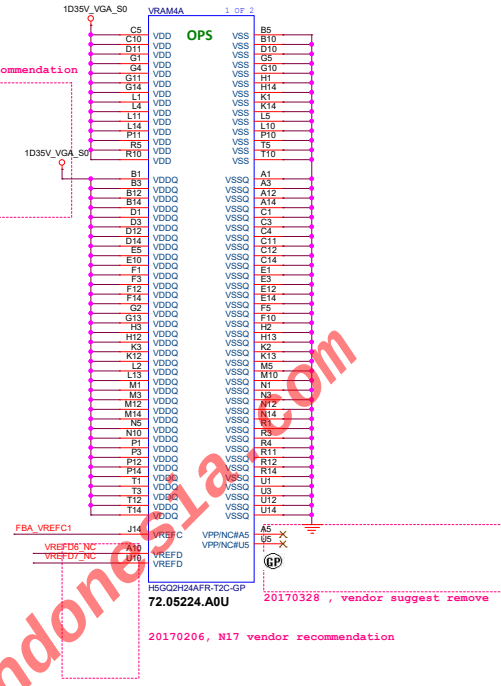


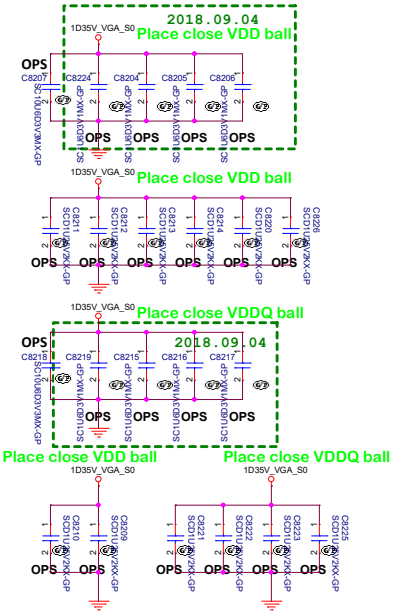
Frame Buffer Patition A-Upper Half

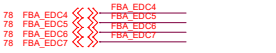


FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low







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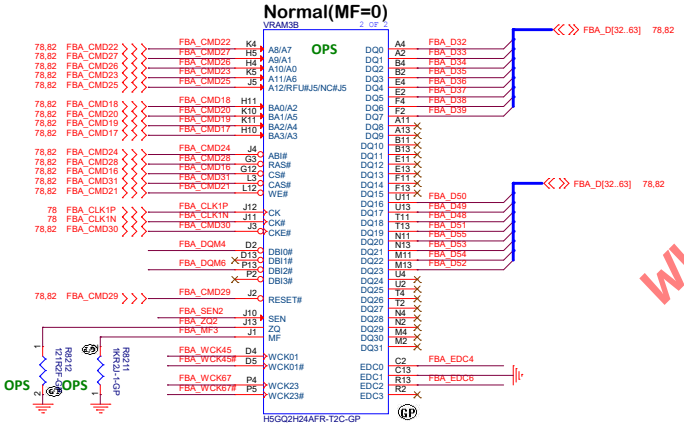

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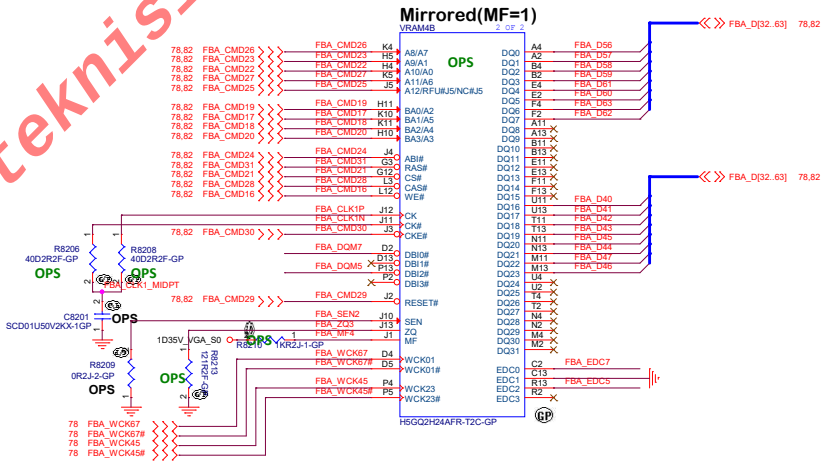

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Title: GPU-VRAM3,4 (2/4)

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Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: BOLT WHL | Rev: A00

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Title: GPU-VRAM7,8 (4/4)

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A3	BOLT WHL	A00

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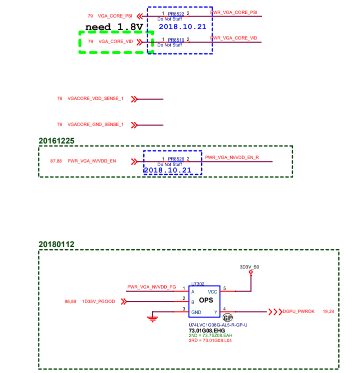
Main FUNC = dGFX CORE

RT8812A/RT8816A For NVVDD



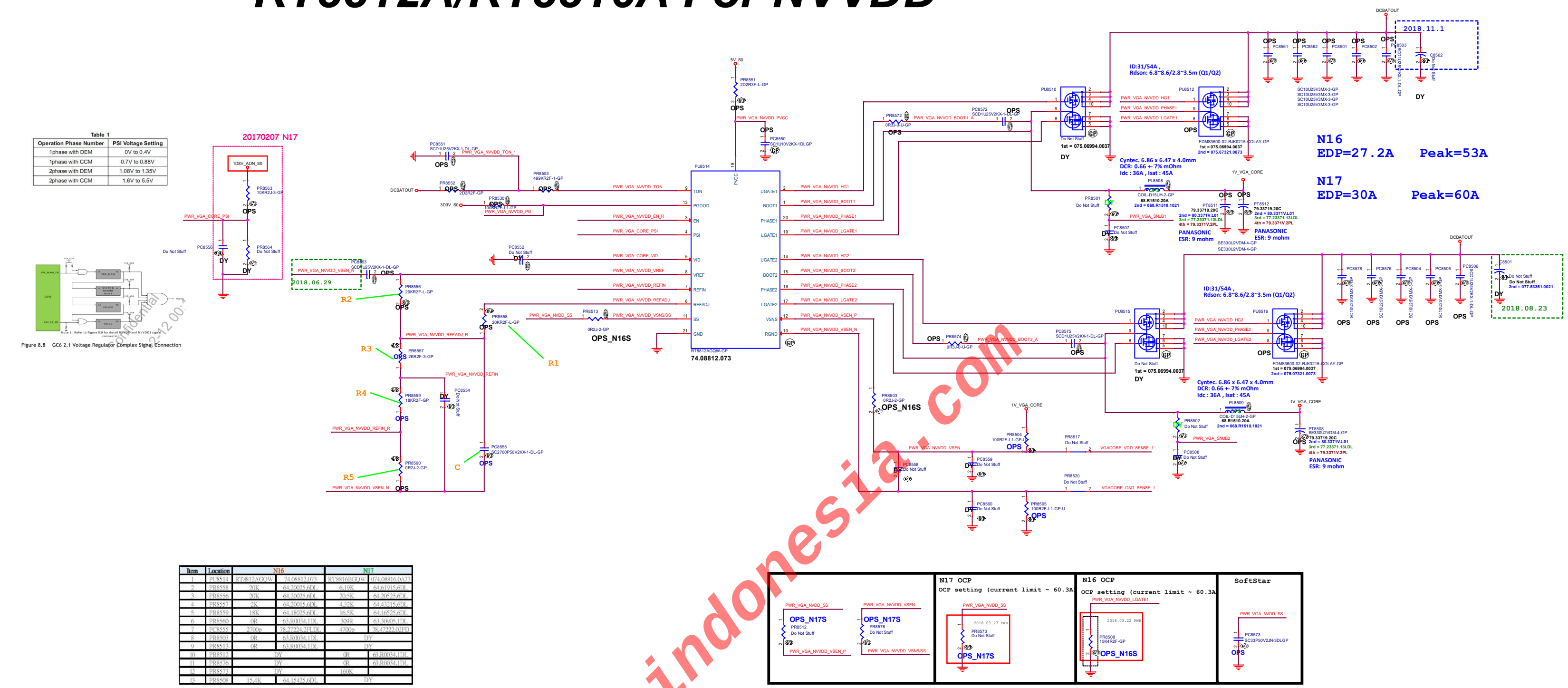


Table 1

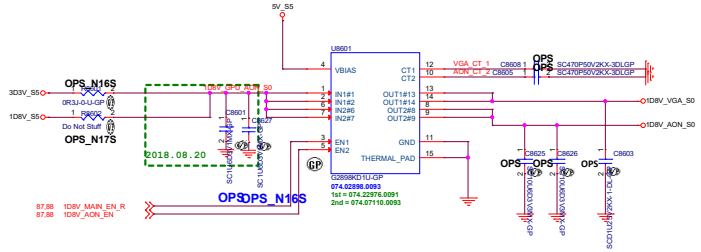
Operation Phase Number	PSI Voltage Setting
1phase with DEM	0V to 0.4V
1phase with CCM	0.7V to 0.88V
2phase with DEM	1.08V to 1.35V
2phase with CCM	1.6V to 5.5V

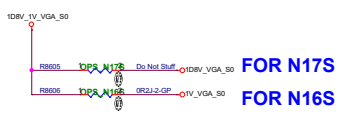
Figure 8.8 GC6 2.1 Voltage Regulator Complex Signal Connection

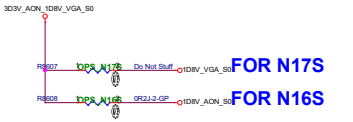
Item	Location	N16		N17	
1	PU8514	RT8812AGQW	74.08812.073	RT8816BGQW	074.08816.0A73
2	PR8558	20K	64.20025.6DL	6.19K	64.61915.6DL
3	PR8556	20K	64.20025.6DL	20.5K	64.20525.6DL
4	PR8557	2K	64.20015.6DL	4.32K	64.43215.6DL
5	PR8559	18K	64.18025.6DL	16.5K	64.16525.6DL
6	PR8560	0R	63.R0034.1DL	309R	63.30905.1DL
7	PC8555	2700p	78.27224.2FLDL	4700p	78.47222.02FD
8	PR8503	0R	63.R0034.1DL	DY	
9	PR8513	0R	63.R0034.1DL	DY	
10	PR8512	DY		0R	63.R0034.1DL
11	PR8576	DY		0R	63.R0034.1DL
12	PR8573	DY		160K	
13	PR8508	15.4K	64.15425.6DL	DY	

VGA Power B

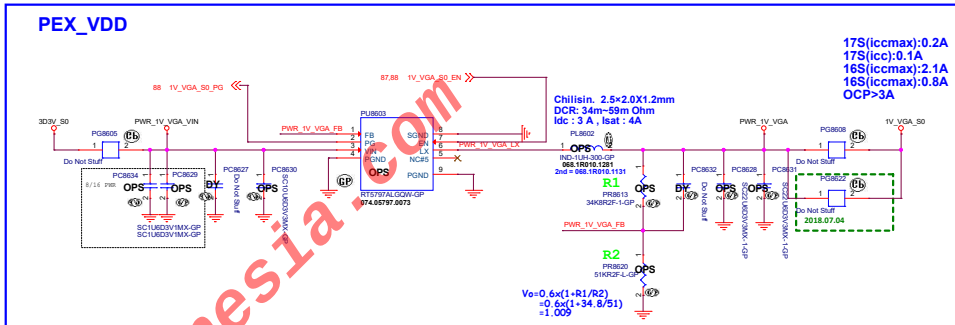
1.8V_VGA_S0
1.8V_AON_S0



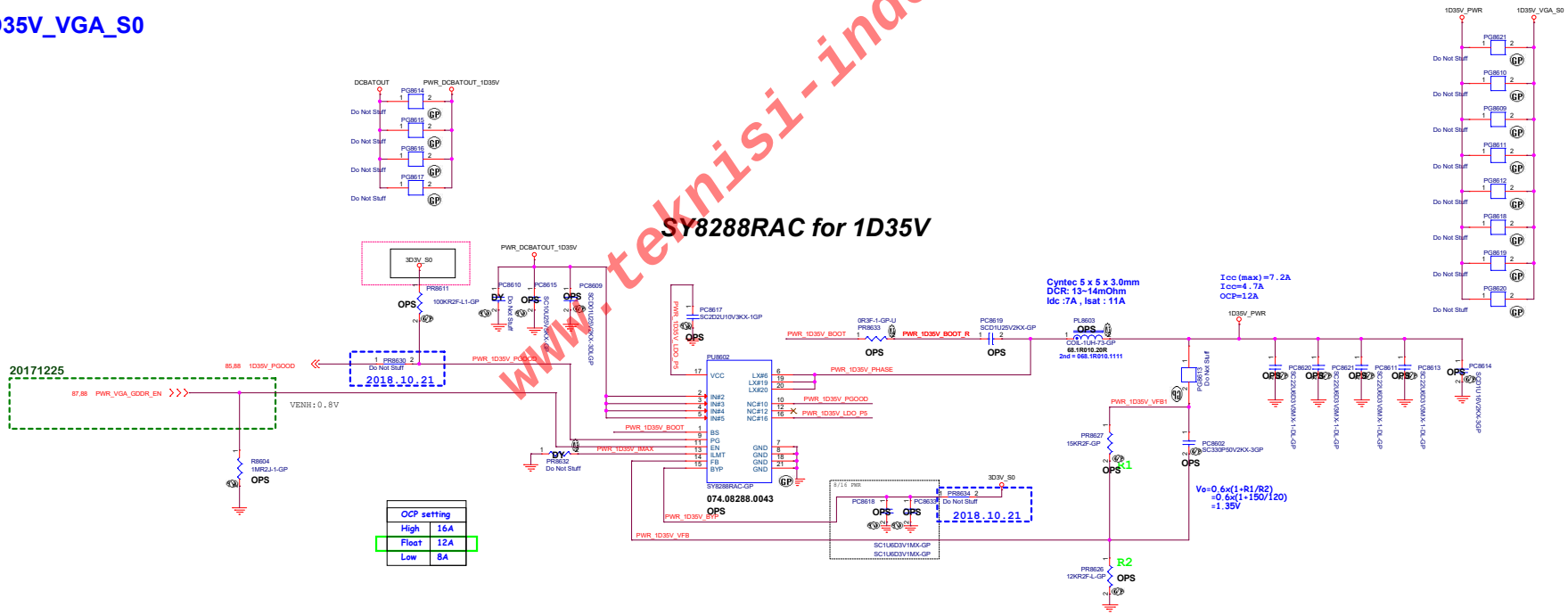




PEX_VDD



1D35V_VGA_S0



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Title: DISCRETE VGA POWER
Size: Custom | Document Number: BOLT WHL | Rev: A00
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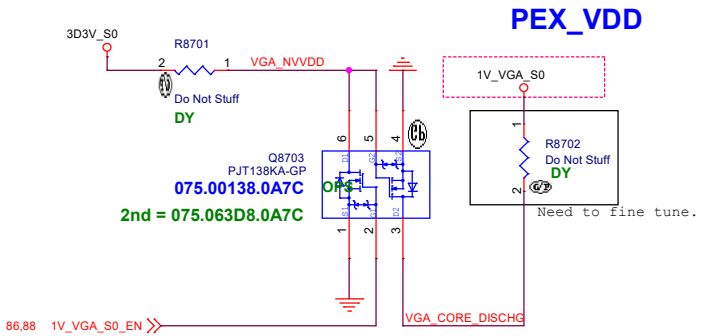

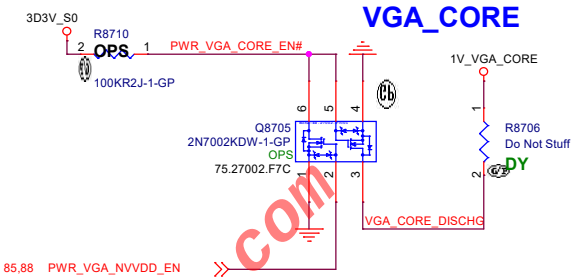

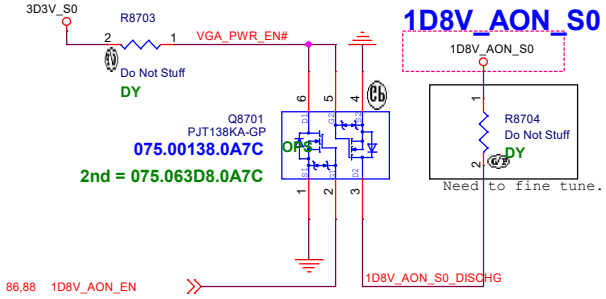

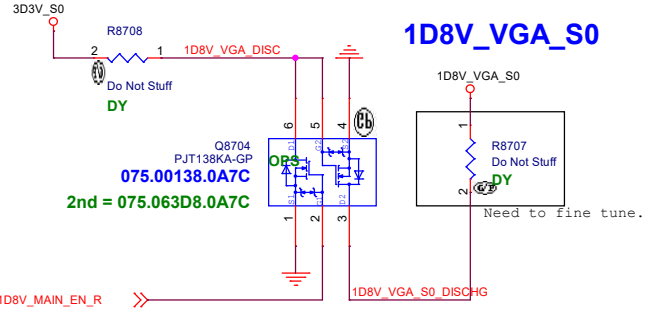

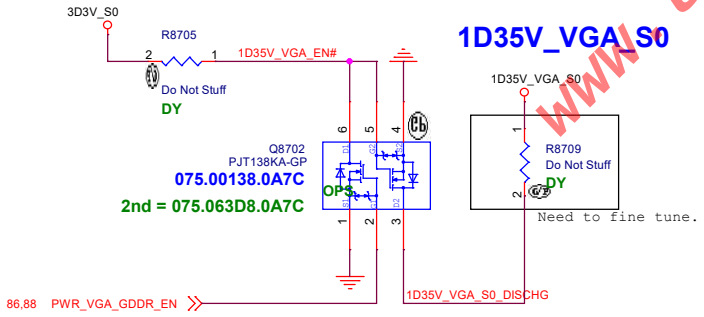

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Title: *Reserved*

Size	Document Number	Rev
A3	BOLT WHL	A00

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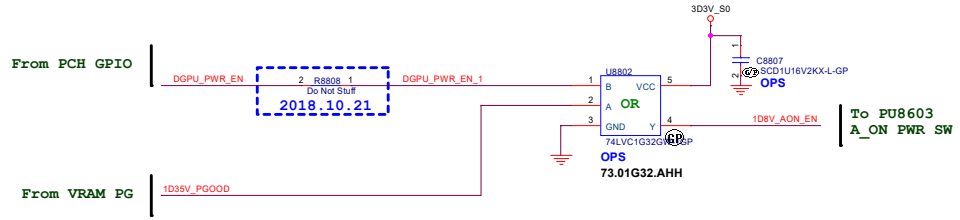
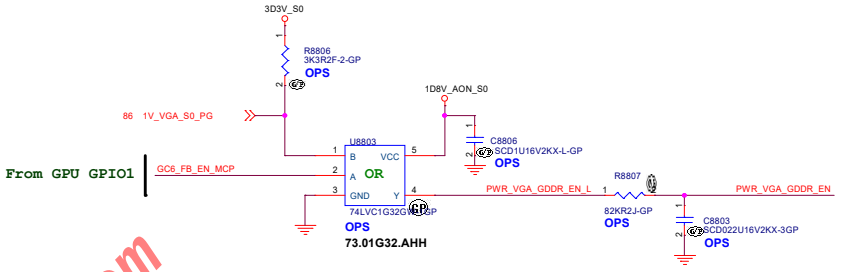
20 DGPU_PWR_EN
85,86 1D35V_PGOOD
86,87 1D8V_AON_EN
79 1D8V_MAIN_EN
86,87 1D8V_MAIN_EN_R
85,87 PWR_VGA_NVVDD_EN
86,87 1V_VGA_S0_EN
20,79 GC6_FB_EN_MCP
86,87 PWR_VGA_GDDR_EN

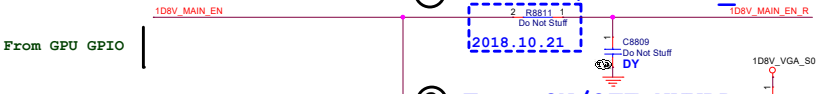
① Turn ON/OFF 1V8_AON



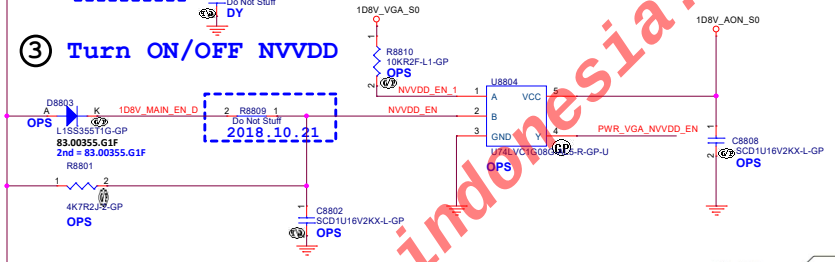
⑤ Turn ON/OFF FBVDD



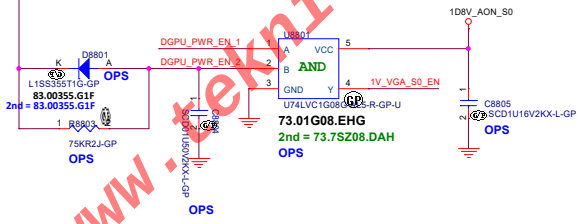
② Turn ON/OFF 1D8V_MAIN

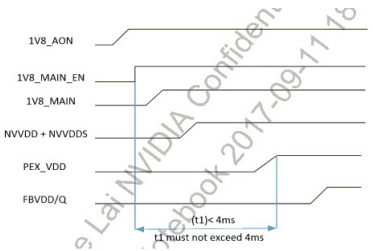


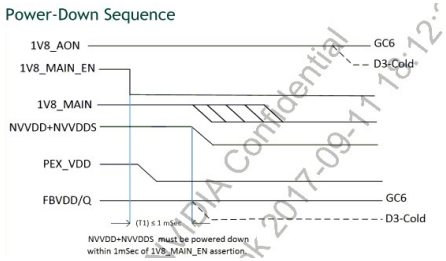
③ Turn ON/OFF NVVDD



④ Turn ON/OFF PEX_VDD







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Title: GPU SEQUENCE

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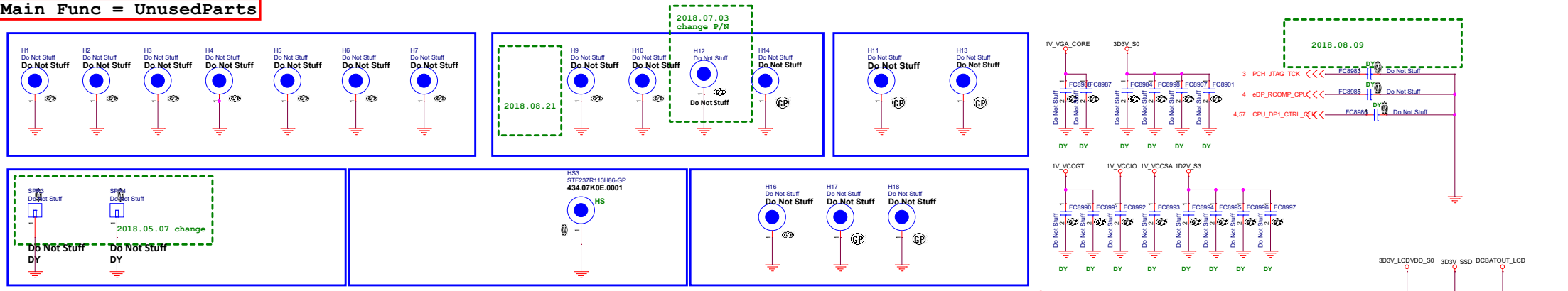
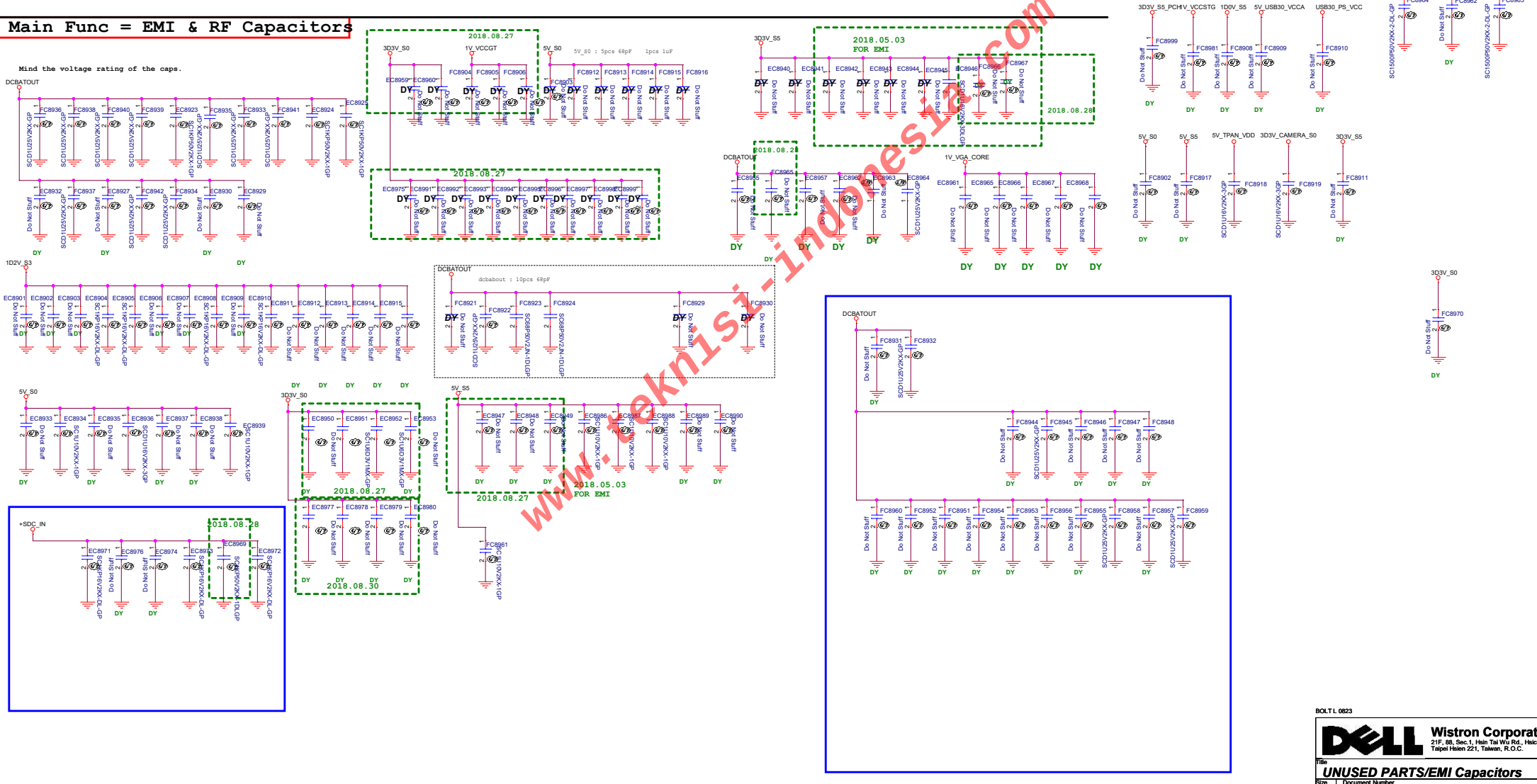
Main Func = UnusedParts



Main Func = EMI & RF Capacitors



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Title: UNUSED PARTS/EMI Capacitors

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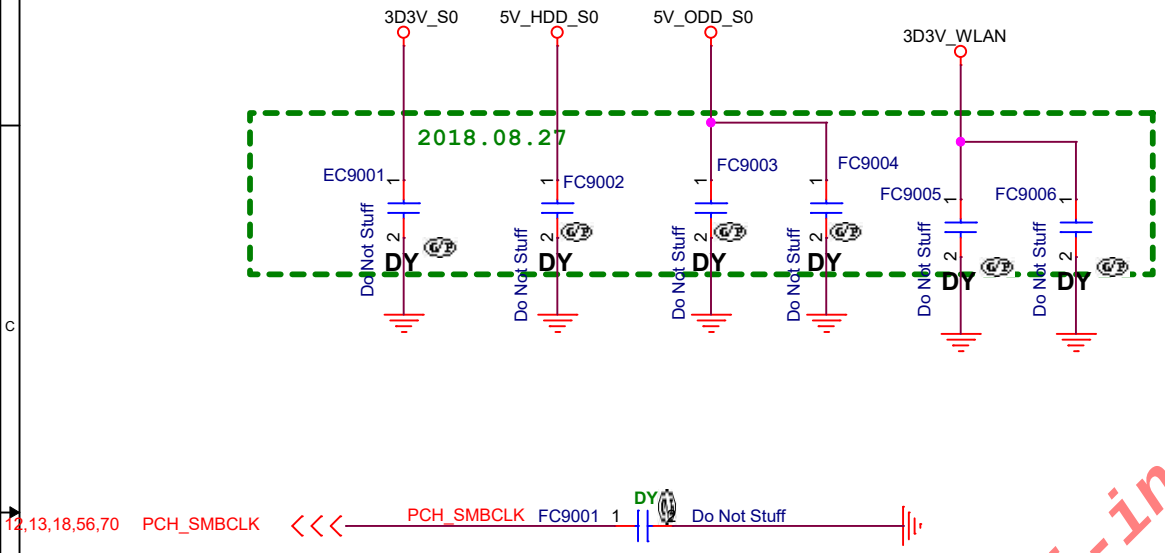

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Title: Reserved

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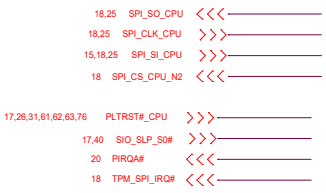
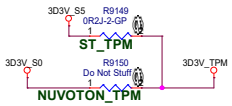
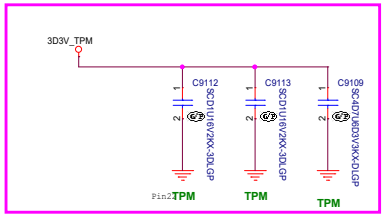
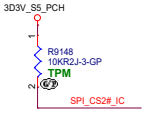
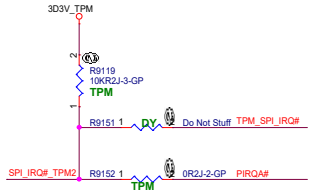
Main Func = TPM

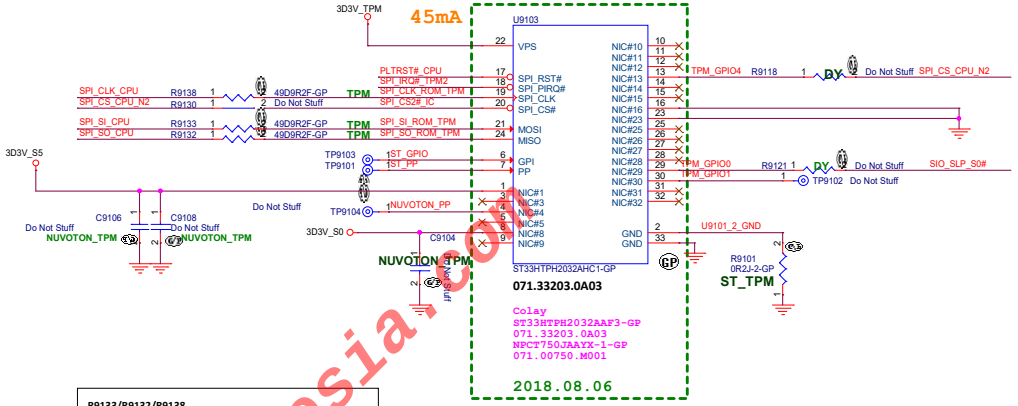












R9133/R9132/R9138		
CPU TYPE	CNL(16M+8M)	WHL(16M)
Bolt_L(TPM)	64.33R05.6DL	64.49R95.6DL
Bolt (non TPM)	DY	DY

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Title: TPM2.0

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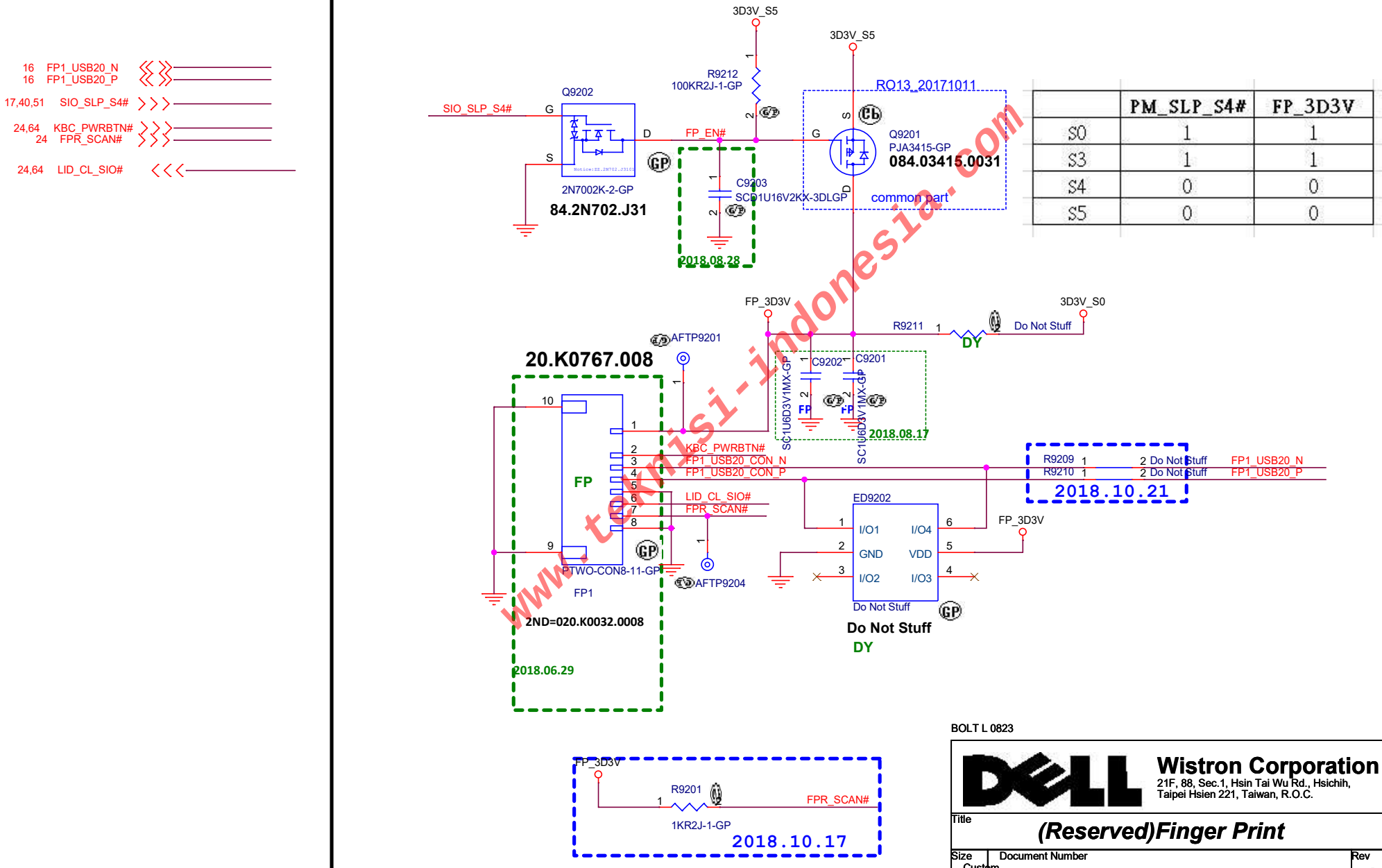
Main FUNC = FPR

FBR(Botton side finger Print Sensor)



	PM_SLP_S4#	FP_3D3V
S0	1	1
S3	1	1
S4	0	0
S5	0	0

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Title

LVDS_Switch

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Title

Firmware SW

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Title: CPU_XDP;PCH_XDP

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A2	BOLT WHL	A00

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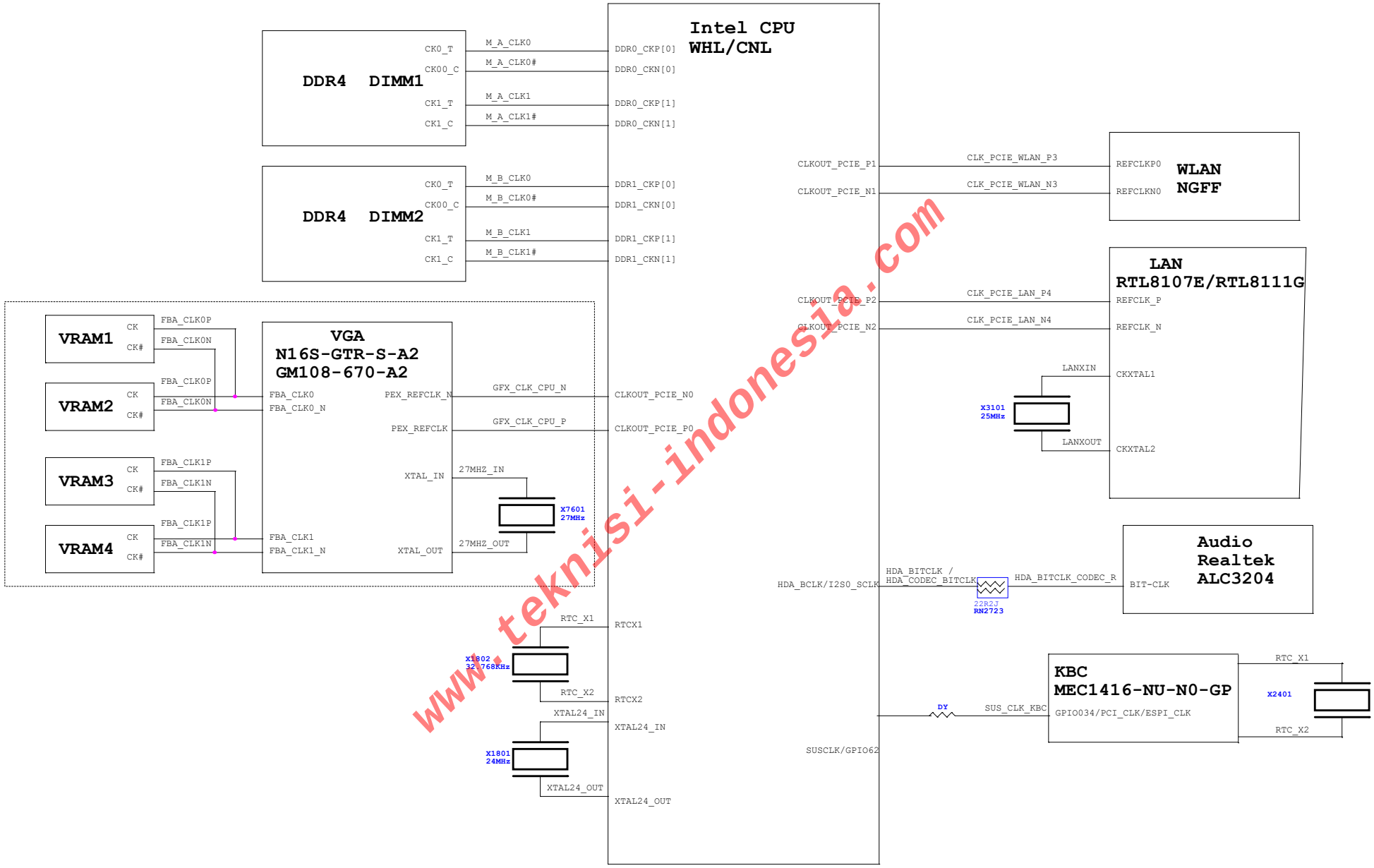
CLK Block Diagram



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Title: CLK Block Diagram

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Change notes -

DATE	VERSON	DATE	Page	Modify List	OWNER

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Title: *Change History*

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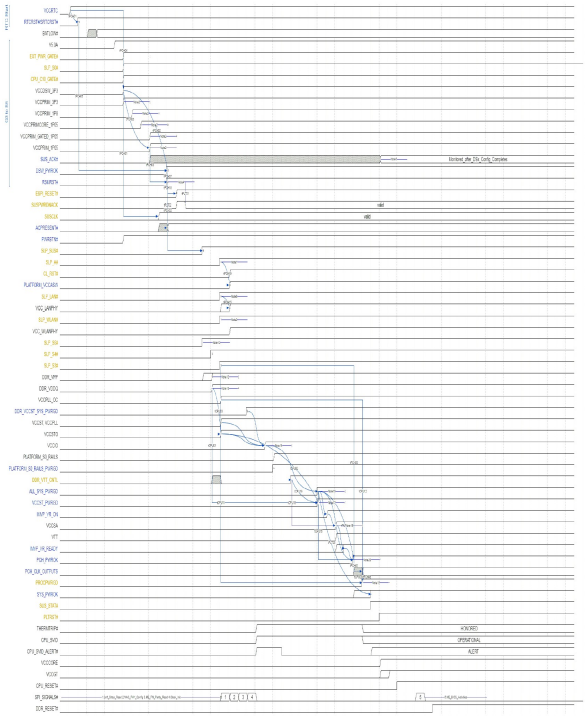
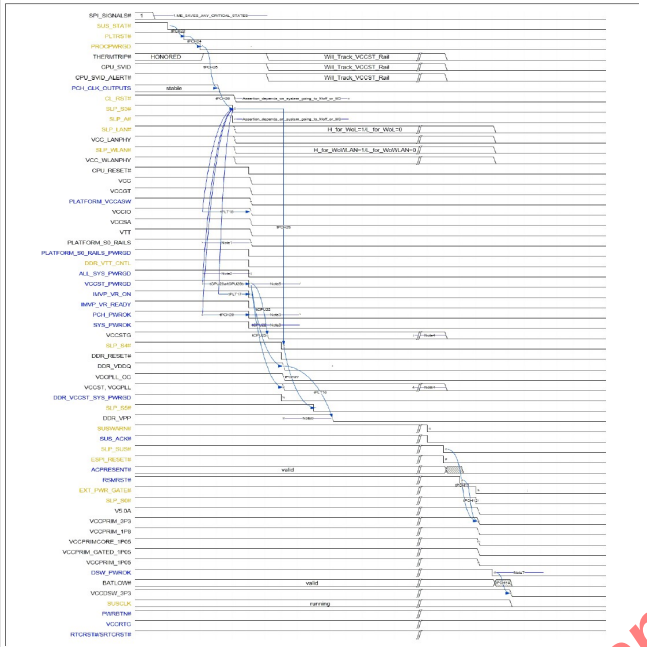
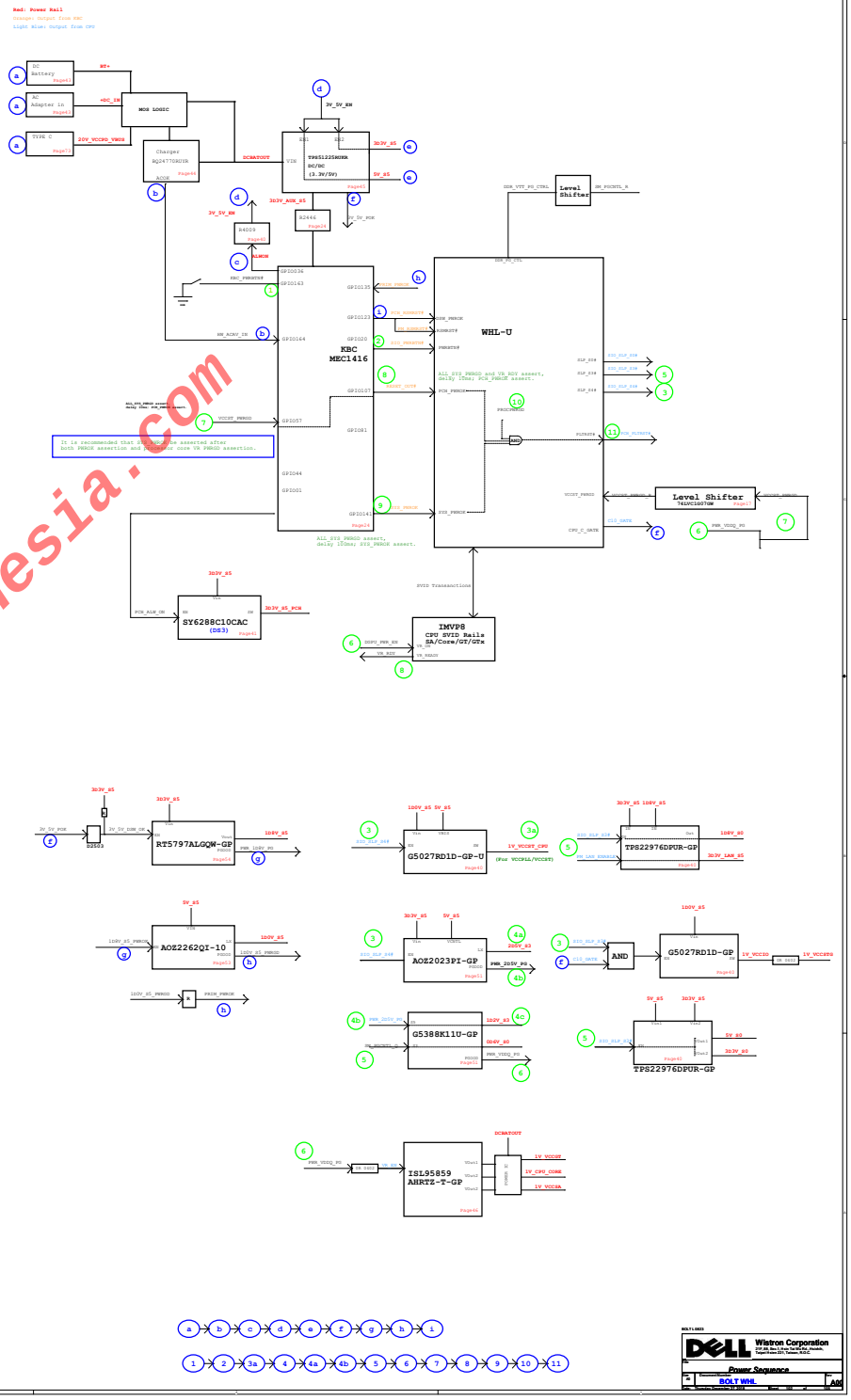
CNL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



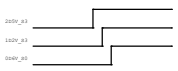
WHL-U/Y Timing Diagram for G3 to S0/M0 [Non Deep Sx Platform]



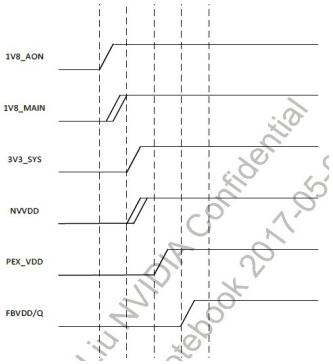
Tulip Skylake POWER UP SEQUENCE DIAGRAM (NON Deep Sx Platform)



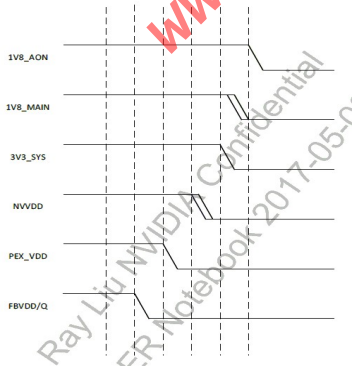
For DDR4 power sequence



NVIDIA GPU Power up sequence



NVIDIA GPU Power down sequence



a → b → c → d → e → f → g → h → i

1 → 2 → 3a → 4 → 4a → 4b → 5 → 6 → 7 → 8 → 9 → 10 → 11

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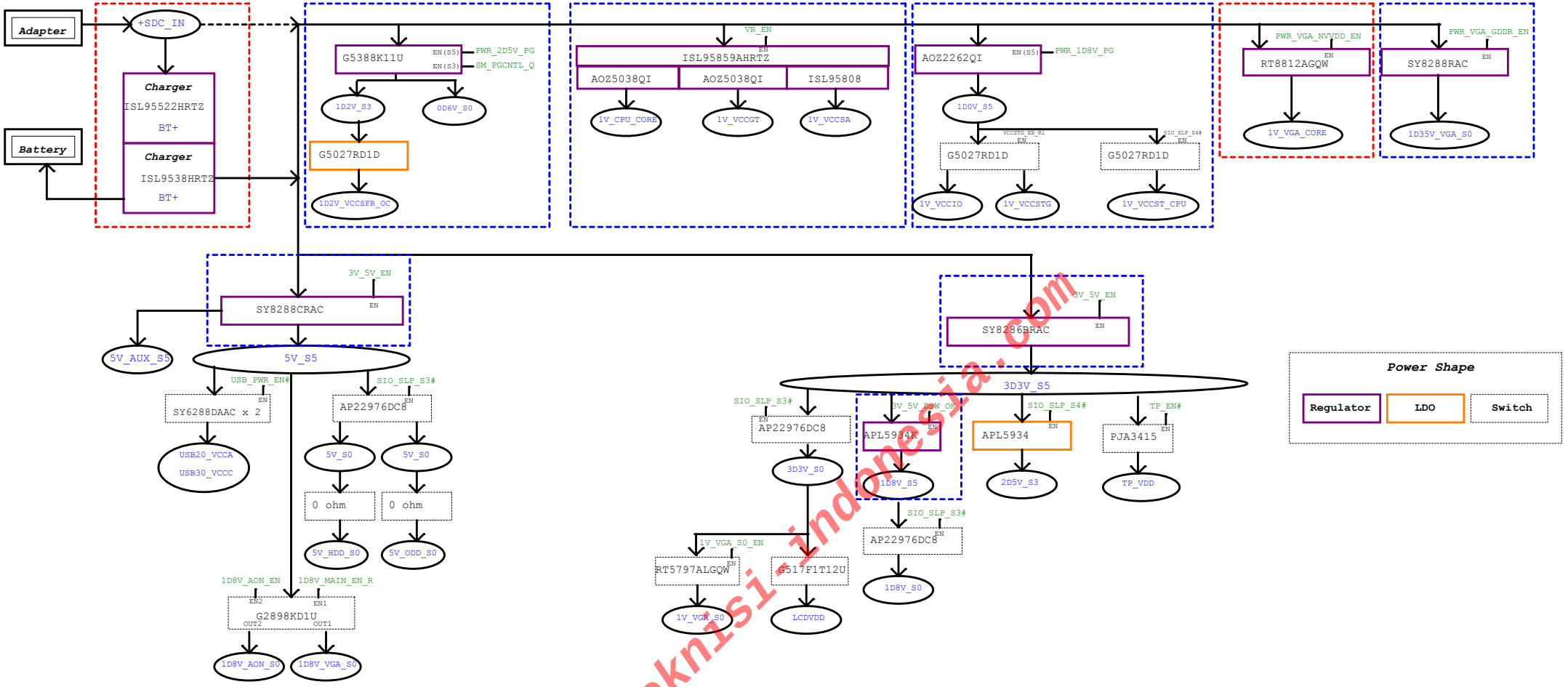
Power Sequence
BOLT WHL



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Title: Power Block Diagram

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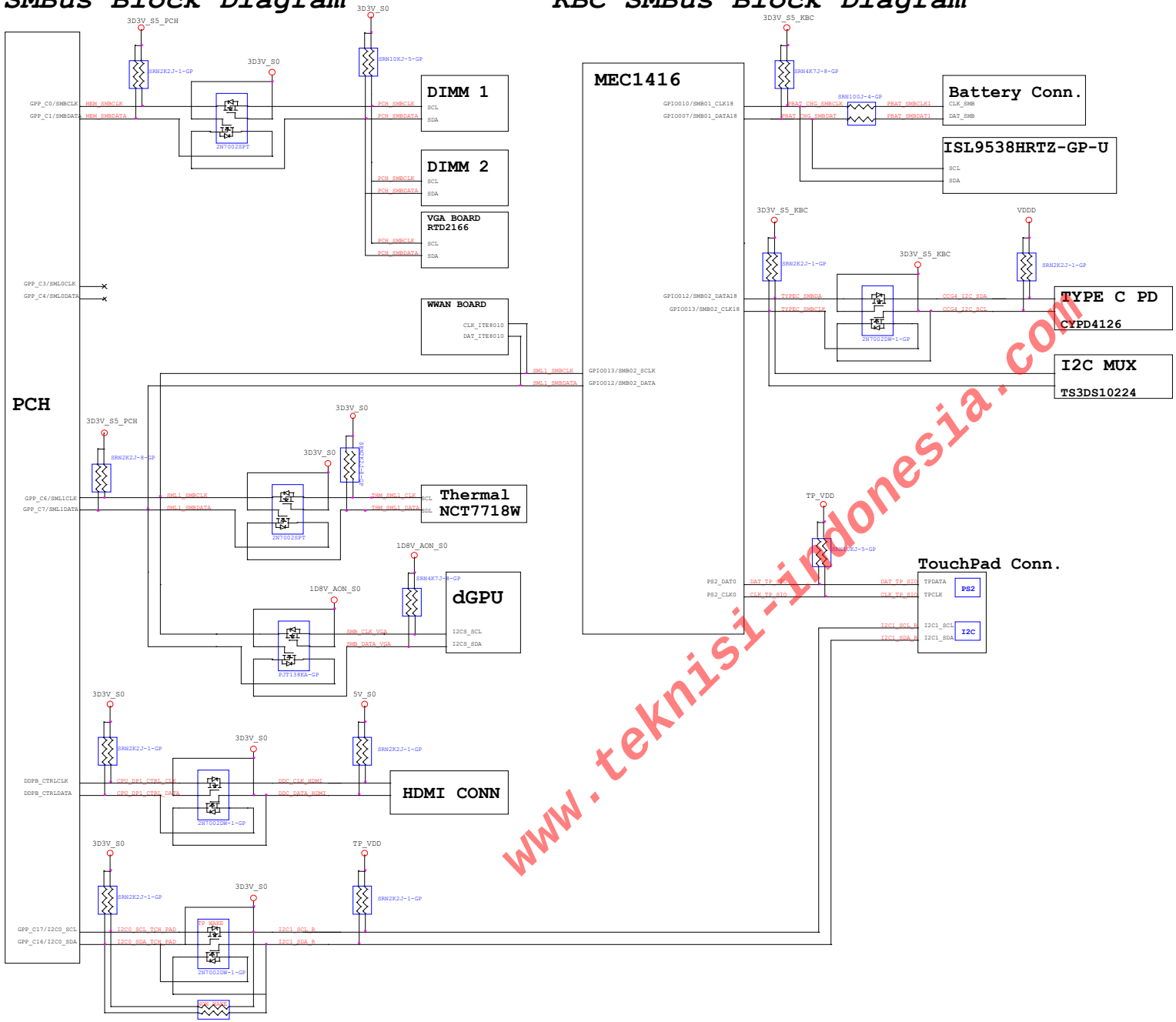
PCH SMBus Block Diagram



KBC SMBus Block Diagram

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Title: SMBUS Block Diagram

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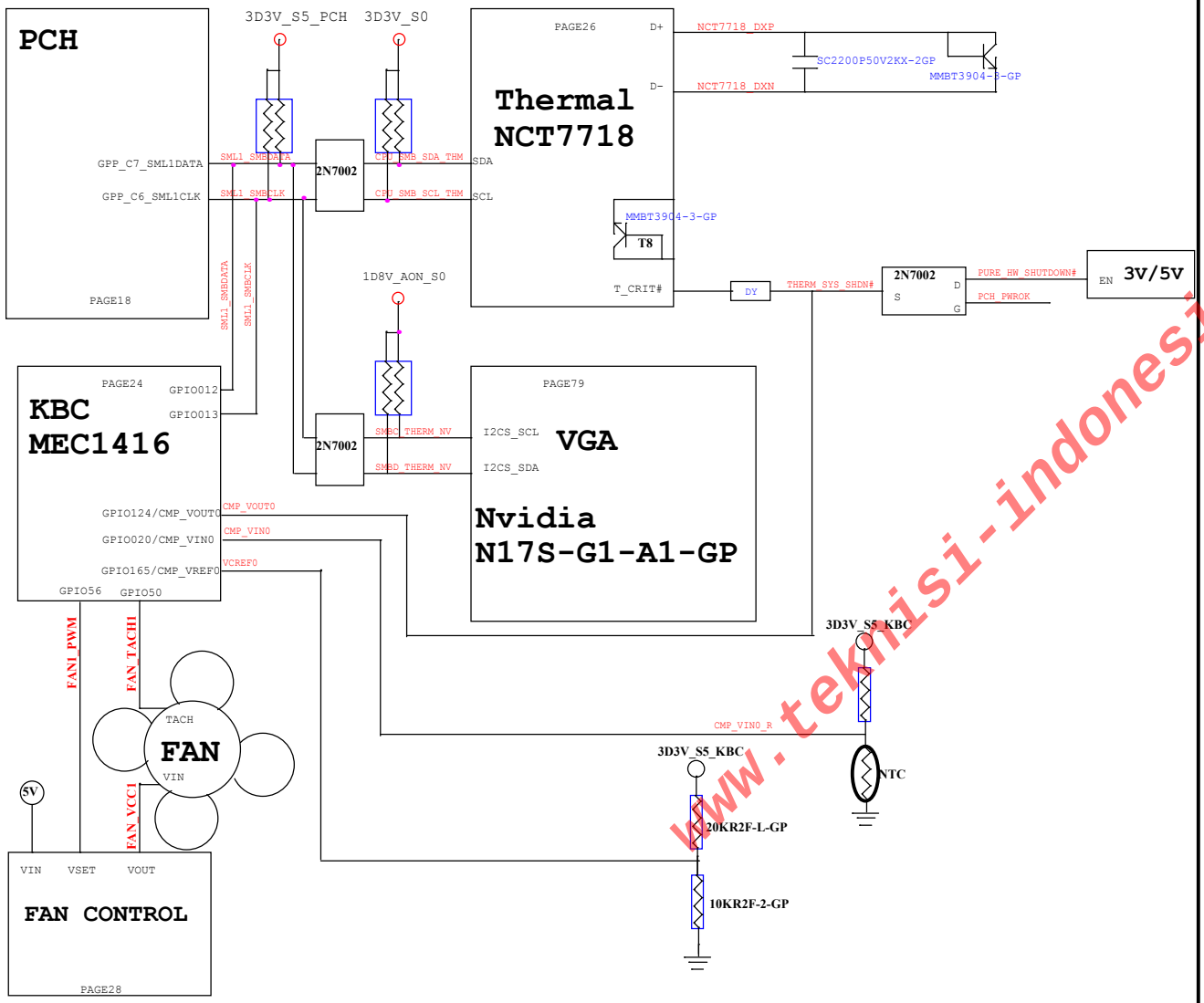
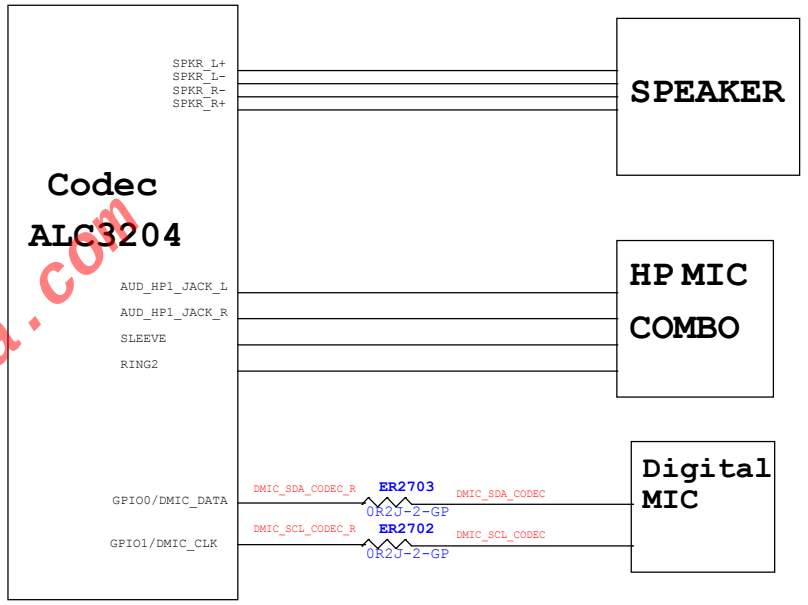
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

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